User's Guide

Agilent Technologies
N5102A Baseband Studio Digital Signal Interface Module

Due to our continuing efforts to improve our products through firmware and hardware revisions, N5102A module design and operation may vary from descriptions in this guide. We recommend that you use the latest revision of this guide to ensure you have up-to-date product information. Compare the print date of this guide (see bottom of page) with the latest revision, which can be downloaded from the following website:

www.agilent.com/find/basebandstudio

Agilent Technologies

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1 Installation

This chapter provides the following:

Safety Information

Warnings, Cautions, and Notes

The following safety notations are used throughout this manual. Familiarize yourself with each notation and its meaning before operating this product.

WARNING	***Warning* denotes a hazard. It calls attention to a condition or situation that could result in personal injury or loss of life. Do not proceed beyond a warning until the indicated conditions or situations are fully understood.**

CAUTION	*Caution* calls attention to a possible condition or situation that could result in a loss of a user's work, damage, or destruction of the product. Do not proceed beyond a caution until the indicated conditions are fully understood.

NOTE	*Note* calls the user's attention to an important point of special information within the text. It provides operational information or additional instructions of which the user should be aware.

Instrument Markings

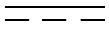
The following markings are is used on the N5102A Baseband Studio digital signal interface module. Familiarize yourself with it and its meaning before operating the module.

The CE mark is a registered trademark of the European Community. If this symbol is accompanied by a year, it is the year when the design was proven.

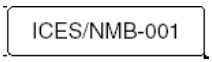
The CSA mark is a registered trademark of the Canadian Standards Association.

The C-Tick Mark is a trademark registered to the Australian Spectrum Management Agency. This indicates compliance with all Australian EMC regulatory information.

This symbol indicates that the center conductor (of the power supply) is positive, and the outer conductor is negative.



This symbol indicates that the input power required is DC.



This symbol indicates compliance with the Canadian Interference-Causing Equipment Standard (ICES-001).

General Safety Considerations

WARNING	**Personal injury may result if the module cover is removed. There are no operator serviceable parts inside. To avoid electrical shock, refer servicing to qualified personnel.**

Getting Started

Checking the Shipment

1. Inspect the shipping container for damage.

   Signs of damage may include a dented or torn shipping container or cushioning material that indicates signs of unusual stress or compacting.

2. Carefully remove the contents from the shipping container and verify that your order is complete.

   The following items are shipped standard with each N5102A Baseband Studio digital signal interface module:

   - user's guide
   - documentation CD-ROM (user's guide and list of SCPI commands)
   - three-prong AC power cord (specific to geographic location)
   - power supply
   - proprietary three-meter digital bus cable
   - five break-out boards (PC boards with connectors that simplify the connections between the N5102A module and the device under test)
   - loop back fixture (for troubleshooting)
   - Device Interface port mating connector
     See "Rear Panel" on page 20 for connector locations.

Instrument Dimensions

Length:	189.9 mm (7.48 in)
Width:	144.8 mm (5.70 in)
Height:	41.6 mm (1.64 in)

Meeting Electrical and Environmental Requirements

The N5102A module is designed for use in the following environmental conditions:

- indoor use
- altitudes < 15,000 feet (4,572 meters)

- 0 to 55°C temperatures, unless otherwise specified
- 80% relative humidity (maximum for temperatures up to 31°C, decreasing linearly to 50% relative humidity at 40°C).

CAUTION This product is designed for use in INSTALLATION CATEGORY II and POLLUTION DEGREE 2, per IEC 61010-1 and 664, respectively.

Ventilation

Ventilation holes are located on the front and rear panels of the N5102A module. Do not allow these holes to be obstructed, as they allow air flow through the module.

When installing the module in a cabinet, the convection into and out of the module must not be restricted. The ambient temperature outside the cabinet must be less than the maximum operating temperature of the module by 4°C for every 100 watts dissipated within the cabinet.

CAUTION Damage to the module may result when the total power dissipated in the cabinet is greater than 800 watts. When this condition exists, forced convection must be applied.

Line Settings

The *N5102A module* requires a power supply that meets the following conditions:

Voltage: 5V

Frequency: DC

Current: 4.0A

The module's *power supply* requires a power source that meets the following conditions:

Voltage: 100–240V

Frequency: 50–60 Hz

Current: 0.7A

CAUTION Damage may result if a supply voltage is not within its specified range.

Connecting the AC Power Cord

This is a Safety Class 1 Product provided with a protective earth ground incorporated into the power cord. The AC power cord is the device that disconnects the mains circuits from the mains supply. In addition, an external circuit breaker, readily identifiable and easily reached by the operator, should be available for use as the disconnecting device. Use the following steps to connect the AC power cord:

WARNING	**Personal injury may occur if there is any interruption of the protective conductor inside or outside of the product. Intentional interruption is prohibited.**

CAUTION	Damage to the product may result without adequate earth grounding. Always use the supplied three-prong AC power cord.

1. Ensure that the power cord is not damaged.
2. Install the product so that one of the following items is readily identifiable and easily reached by the operator: AC power cord, alternative switch, or circuit breaker.
3. Insert the mains plug into a socket outlet provided with a protective earth grounding.

AC Power Cord Localization

The AC power cord included with the module is appropriate for the final shipping destination. You can, however, order additional AC power cords for use in different areas: see “Replaceable Parts” on page 112.

Proper Usage and Cleaning

The N5102A module cover protects against physical contact with internal assemblies that contain hazardous voltages, but does not protect against the entrance of water. To avoid damage and personal injury, ensure that liquid substances are positioned away from your N5102A module.

WARNING	**Personal injury may result if the N5102A module is not used as specified. Unspecified use impairs the protection provided by the equipment. The N5102A module must be used with all means for protection intact.**

Cleaning Suggestions

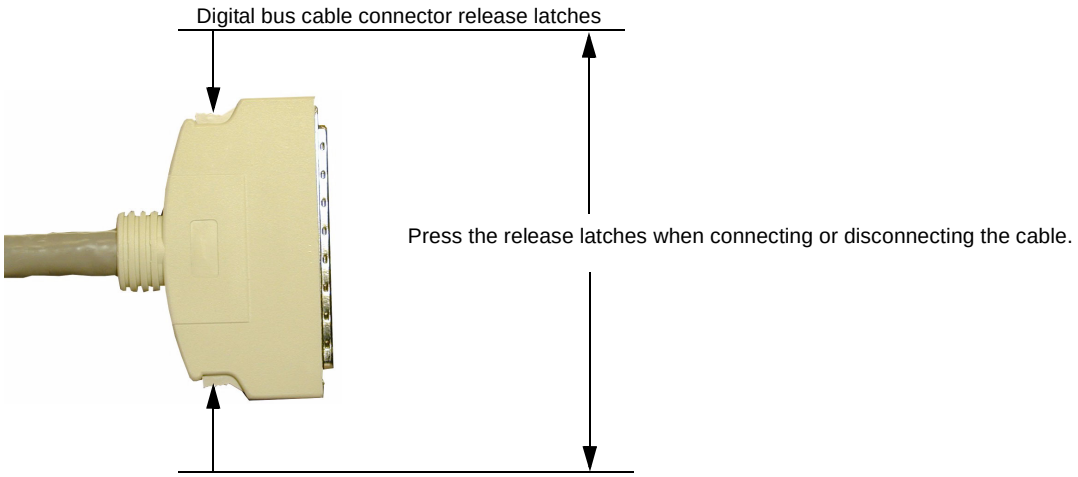
To prevent dust build-up that could potentially obstruct ventilation, clean the N5102A module cover periodically. Use a dry cloth, or one slightly dampened with water, to clean the external case parts.

WARNING **Electrical shock may result if the N5102A module is not disconnected from the mains supply before cleaning. Do not attempt to clean internally.**

Connecting the N5102A Module to the ESG/PSG

The N5102A module is used with an Agilent E4438C ESG[1] or E8267C PSG[2] signal generator. This section provides information on connecting the N5102A module to the signal generator. While the graphics show an ESG signal generator, the procedure is the same for the PSG.

CAUTION The digital bus cable connector has a release latch on each side (as shown below). To avoid connector damage, simultaneously squeeze both release latches when connecting or disconnecting the cable. A securely connected cable does not come loose when gently pulled.



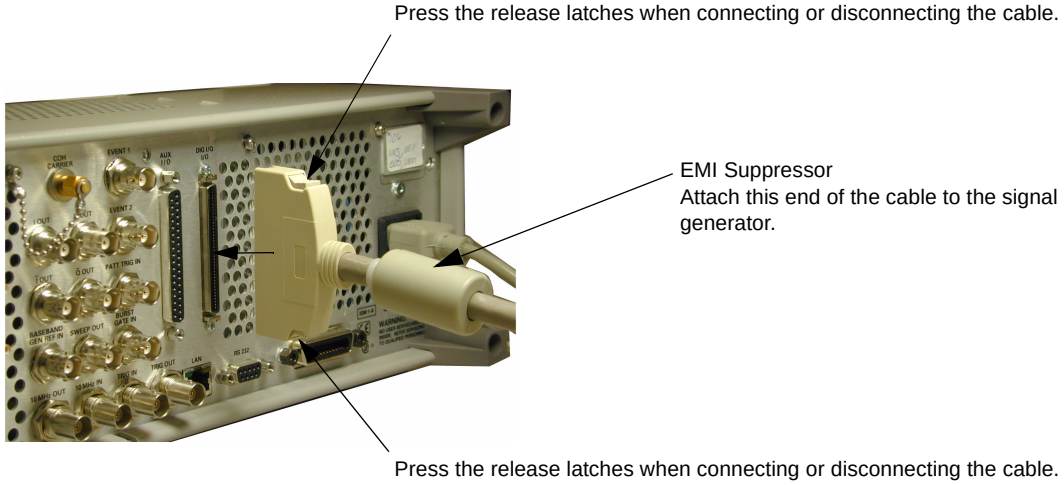
1. Refer to Figure 1-1. Connect the end of the digital bus cable that has the EMI suppressor to the signal generator's rear panel digital bus connector.

[1]Requires Options 003 and/or 004, and either 601 or 602.

[2]Requires Options 003 and/or 004, and 602.

NOTE The digital bus connector may be labeled as DIGITAL BUS, DIG I/Q I/O, or DIGITAL I-Q I/O.

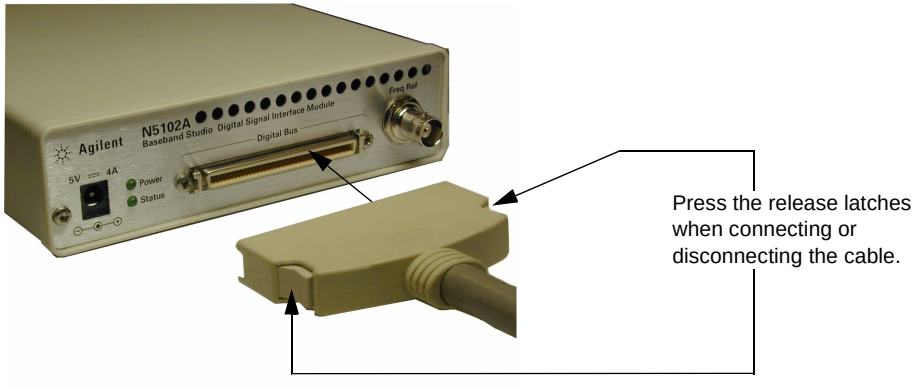
Figure 1-1 Signal Generator Digital Bus Cable Connection



2. Refer to Figure 1-2. Connect the other end of the digital bus cable to the Digital Bus connector on the N5102A module.

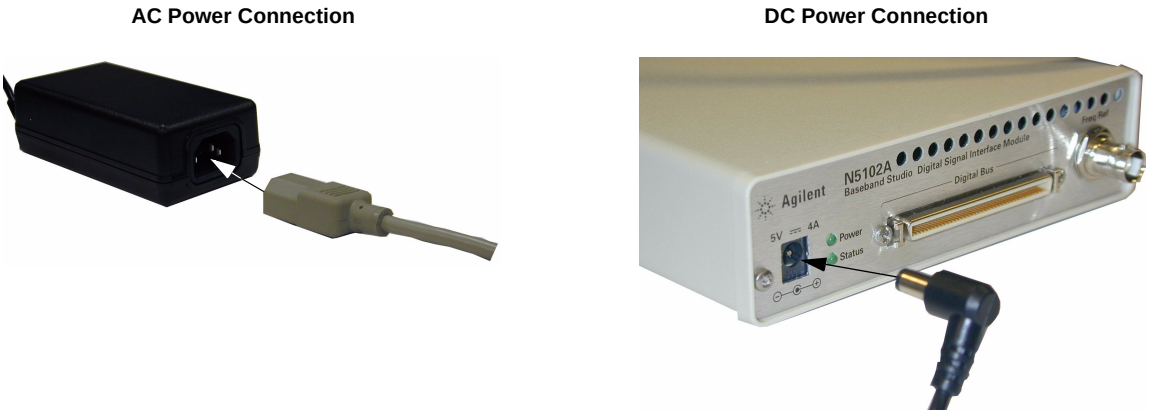
   The proprietary three meter cable enables you to place the interface module in a location close to the device under test (DUT).

Figure 1-2 N5102A Module Digital Bus Cable Connection



3. Refer to Figure 1-3. Connect the AC power cord to both the power supply and the AC power source (for details on connecting an AC power cord to an AC power source, see "Connecting the AC Power Cord" on page 6).
4. Connect the power supply to the N5102A module DC power receptacle.

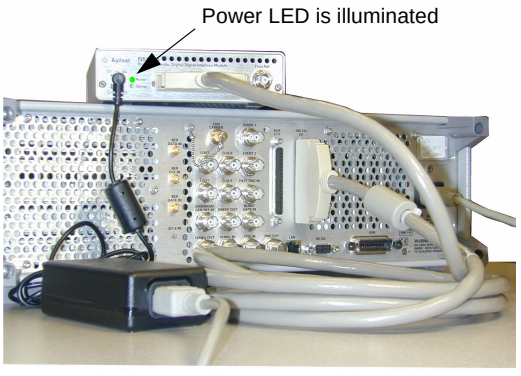
Figure 1-3 N5102A Module Power Supply Connections



The power LED should be illuminated, indicating that the interface module is connected to the power source. If the power LED is not illuminated, check the AC power connection for the power supply and ensure that the DC power supply plug is fully inserted into the N5102A module DC power receptacle. If problems still persist after checking the power cords, refer to Chapter 6, "Troubleshooting," on page 105.

Figure 1-4 shows a completed installation.

Figure 1-4 Completed N5102A Module Installation



Operation Verification

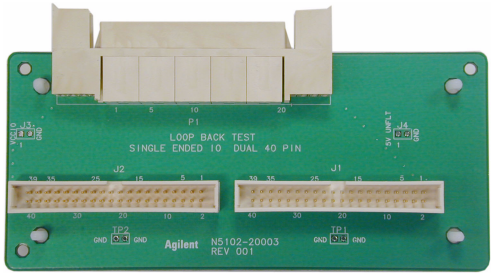
The N5102A module is configured and controlled using the user interface (UI) on the ESG/PSG signal generator. The operation verification uses the device interface test (Device Intfc), which is one of four interface module diagnostic tests, referred to as loop back tests. This loop back test checks the complete setup, providing a high level of confidence that the system is functioning properly. The three other tests are used if this test fails, and are described in "Running Diagnostic Tests" on page 108.

CAUTION The Device Interface connector on the interface module communicates using high speed digital data. Use ESD precautions to eliminate potential damage when making connections.

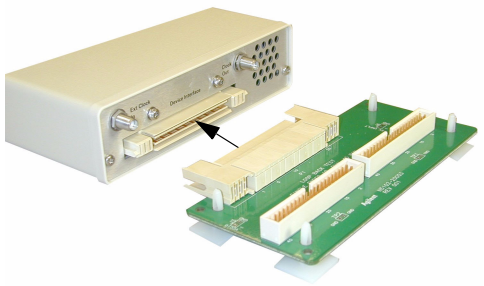
1. Connect the N5102A module to the signal generator (as described in "Connecting the N5102A Module to the ESG/PSG" on page 8).
2. Refer to Figure 1-5. Connect the Loop Back Test Single Ended IO Dual 40 Pin board to the Device Interface connector on the rear panel of the N5102A module.

Figure 1-5 Connecting the Loop Back Board to the N5102A Module

Loop Back Test Single Ended IO Dual 40 Pin Board



Connecting the Board to the Device Interface Connector



The Loop Back Test Single Ended IO Dual 40 Pin board is used both for loop back testing, and as a break-out board to simplify the connection between the N5102A module and the device under test. When used for loopback testing, there should be no connections to the dual 40-pin connectors.

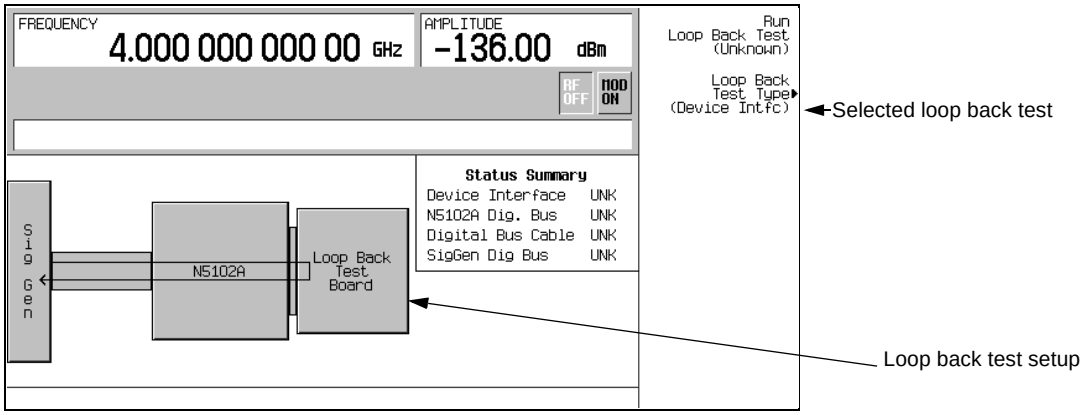
3. If the signal generator is not already on, turn it on.

4. On the signal generator, select the device interface test:

   Press **Aux Fctn** > **N5102A Interface** > **Diagnostics** > **Loop Back Test Type** > **Device Intfc**.

   As shown in Figure 1-6, the currently selected test is displayed in parenthesis below the **Loop Back Test Type** softkey. Note also that the graphic provided displays the current test setup.

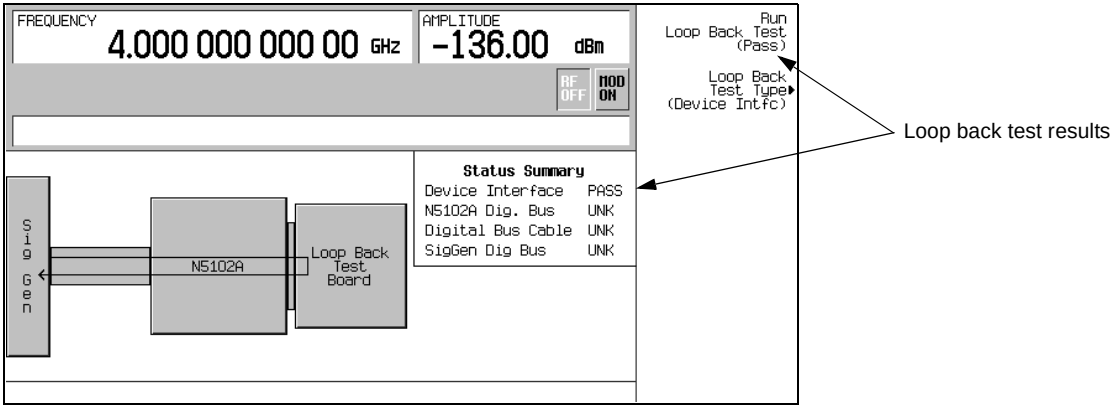
Figure 1-6 ESG/PSG Diagnostic Test Display



5. Run the selected test: press **Run Loop Back Test**.

   When the test completes, the results of the test (pass or fail) replaces `Unknown` in both the parenthesis with the softkey and in the `Status Summary` display as shown in Figure 1-7. If this test fails, refer to "Running Diagnostic Tests" on page 108.

Figure 1-7 ESG/PSG Loop Back Test Result



Regulatory Information

Statement of Compliance

This product has been designed and tested in accordance with IEC Publication 61010, *Safety Requirements for Electronic Measuring Apparatus*, and has been supplied in a safe condition. The documentation contains information and warnings that must be followed by the user to ensure safe operation and to maintain the product in a safe condition.

Assistance

Product maintenance agreements and other customer assistance agreements are available for Agilent Technologies products. For any assistance, contact Agilent Technologies (see page 113).

Certification

Agilent Technologies certifies that this product met its published specifications at the time of shipment from the factory.

- this product does not require calibration

Declaration of Conformity

A declaration of conformity is on file for this product, and a copy is available upon request.

Compliance with German Noise Requirements

This is to declare that this instrument is in conformance with the German Regulation on Noise Declaration for Machines (Laermangabe nach der Maschinenlaermrerordnung –3.GSGV Deutschland).

Table 1-1 German Noise Requirements

Acoustic Noise Emission/Geraeuschemission	
LpA < 70 dB	LpA < 70 dB
Operator position	am Arbeitsplatz
Normal position	normaler Betrieb
per ISO 7779	nach DIN 45635 t.19

Compliance with Canadian EMC Requirements

This ISM device complies with Canadian ICES-001.
Cet appareil ISM est conforme a la norme NMB du Canada.

2 Overview

This chapter describes the features of the N5102A Baseband Studio digital signal interface module along with the signal generator options required for its operation.

Features

The N5102A Baseband Studio digital signal interface module works with the Agilent E4438C ESG[1] or E8267C PSG[2] vector signal generators to provide a flexible digital interface for delivering digital baseband (IQ) or digital intermediate frequency (IF) test signals. The complex modulation formats of the signal generators, including W-CDMA, multitone, 1xEV-DV, WLAN and many more, are available at the bit level for testing digital components, transceivers, and subsystems. The N5102A module delivers the digital IQ or digital IF[3] signals to your device with the data requirements, clock features, and signaling you need. With its selection of logic types and break-out board connectors, the interface module connects into your test system, in most cases eliminating the need for custom fixtures.

The N5102A module provides many features:

- output mode (requires Option 003)
- input mode (requires Option 004)
- bit level access to arbitrary waveform generator (ARB) and real-time signal generator baseband data from a wide range of signal creation applications
- simple user interface
- flexible data formats
  - — variable 4-bit to 16-bit word size
  - — serial, parallel, and parallel interleaved data transmission
  - — 2's complement or offset binary word representation
  - — MSB or LSB bit order
  - — digital IQ or digital IF[3] signal
- flexible clocking
  - — automatic resampling
  - — 1 kHz to 100 MHz sample rate
  - — multiple clock inputs and outputs
  - — adjustable clock phase and skew

[1]Requires either Option 601 or 602.

[2]Requires Option 602.

[3]Digital IF only available for output mode.

  - — multiple clocks per sample 1x, 2x, and 4x (Output mode only. Input mode is limited to 1x.)

- flexible signal interface
  - — multiple logic types provide single ended and differential testing capability—low voltage TTL (LVTTL), LVDS, and CMOS 1.5 V, 1.8 V, 2.5 V, and 3.3 V
  - — proprietary three meter digital bus cable connects the N5102A module to the signal generator
  - — interchangeable break-out boards

The parameters for the N5102A module are set using the UI on the ESG/PSG signal generators. This provides familiar softkey operation for both the modulation format and the interface module. Option 003 (output mode) and Option 004 (input mode) on the ESG/PSG enable the N5102A module user interface on the signal generators.

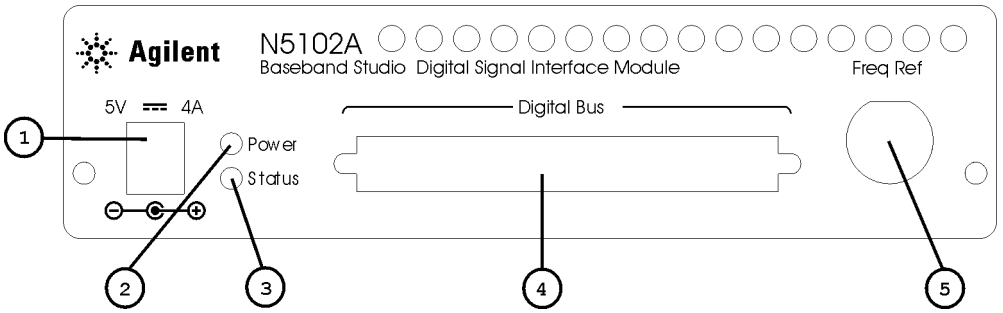
With the N5102A module connected to the signal generator, you can perform multiple levels of testing. Since the baseband data that is provided to the interface module is the same data that can be modulated onto the RF carrier, this enables early-stage testing of digital components and subsystems with the N5102A module, and then testing the integrated system using the modulated RF carrier.

The N5102A digital interface module does not support the Real Time GPS format.

Front Panel

The baseband data and frequency reference inputs for the N5102A module are located on the front panel along with the receptacle for the DC power. A Power LED indicates when DC power has been applied and a Status LED shows when the data lines are active.

Figure 2-1 Front Panel Features



1. DC Power Receptacle

This receptacle accepts the DC power cord from the power supply. A DC power cord is shipped with the interface module.

2. Power LED

This LED illuminates when DC power is supplied to the N5102A module.

3. Status LED

This LED illuminates when the interface module is first turned on by pressing the **N5102A Off On** softkey located in the signal generator UI or after performing a module diagnostic test. Once lit, the LED stays on until the DC power is removed from the interface module. The LED conveys the status of the data lines and has two modes of operation:

Blinks Rapidly	This indicates that the data lines are active and ready to transmit or are transmitting a digital signal.
Solid Illumination	The data lines are inactive.

4. Digital Bus Connector

The N5102A module uses this connector to communicate with the ESG/PSG signal generator. A proprietary three-meter digital bus cable is supplied that connects to the Digital Bus connector.

5. Freq Ref Connector

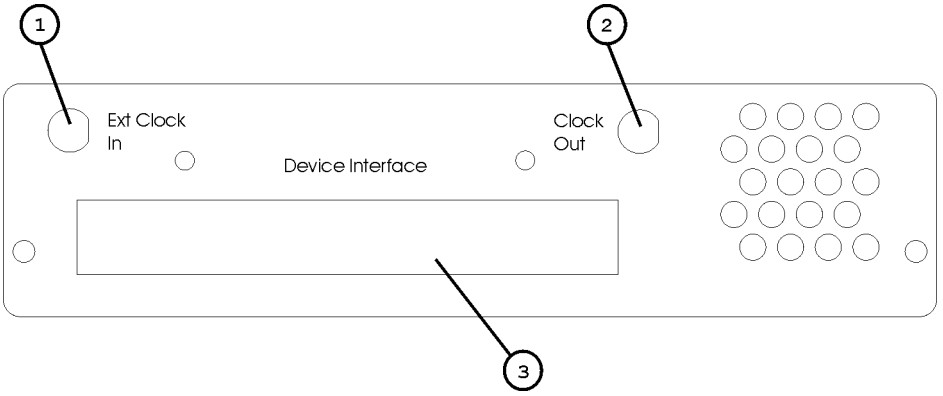
When Internal is the selected clock source, the clock is referenced to this 50Ω connector. This connector accepts an external clock at 3 dBm ±6 dB within the frequency range of 1 MHz to 100 MHz.

CAUTION It is important that the signal generator, the interface module, and the DUT are locked to a common frequency reference. Failure to have a common frequency reference may result in a loss of data. See "Common Frequency Reference" on page 48 for information.

Rear Panel

The rear panel has three connectors that are shown in Figure 2-2 and are described in the following sections.

Figure 2-2 Rear Panel Features



1. Ext Clock In Connector

This AC coupled 50Ω connector is used for connecting an external clock source to the N5102A module. It accepts a signal with a nominal amplitude of 0 dBm and has a frequency range of 1 MHz to 400 MHz.

CAUTION It is important that the signal generator, the interface module, and the DUT are locked to a common frequency reference. Failure to have a common frequency reference may result in a loss of data. See "Common Frequency Reference" on page 48 for information.

2. Clock Out Connector

This 50Ω connector outputs the clock signal at a nominal 400 mV_{p-p} level with a frequency range of 100 kHz to 400 MHz. For a frequency range of 1 kHz to 100 kHz, a high impedance load of 5 kΩ produces a nominal 2 V_{p-p} clock signal.

3. Device Interface Connector

This connector interfaces with the device under test and supplies the digital IQ and digital IF signals in addition to sense lines, ground connections, a DC supply, and input and output clock signals. For more information on this connector, including a pin-out diagram, see “Device Interface Connector” on page 34.

CAUTION The Device Interface connector on the interface module communicates using high speed digital data. Use ESD precautions to eliminate potential damage when making connections.

3 Device Interface Connections

This chapter provides information for the N5102A module Device Interface connector, the supplied break-out boards, and the device interface mating connector.

Break-Out Boards

This section describes the different break-out boards and provides pin-out diagrams for each one.

To maximize signal integrity, make the device connection as close as possible to the N5102A module Device Interface connector. The break-out boards are supplied to aid in minimizing this distance. An alternate solution is to incorporate the device interface mating connector onto the device under test (DUT). This eliminates the need for the break-out board and connecting cables.

Five interchangeable break-out boards are supplied with the N5102A module, each with a different type of connector, providing a wide range of connection possibilities. The break-out boards connect to the Device Interface connector on the rear panel of the module. The different boards are easily identified by their connector. If the situation arises where none of the break-out boards mate with the device being tested, make a customize connection solution using the device interface mating connector. See "Device Interface Connector" on page 34 and "Device Interface Mating Connector" on page 39 for information. Table 3-1 lists the five break-out boards and the test type for which each is intended.

Table 3-1 Break-Out Board List

Break-Out Board	Test Type	Comment
Single Ended I/O Dual 20 Pin	Single-ended	0.1 inch spaced header This connector is commonly used for Agilent logic analyzer probe connections.
Differential I/O Dual 38 Pin	Differential	This connector is commonly used for Agilent logic analyzer probe connections.
Loop Back Test Single Ended IO Dual 40 Pin	Single-ended	0.1 inch spaced header This board serves a dual purpose: • as a break-out board for DUT connectivity • used for N5102A module diagnostic testing
Single Ended I/O 68 Pin	Single-ended	Single SCSI style connector
Differential I/O Dual 100 Pin	Differential	This connector is commonly used for Agilent logic analyzer probe connections.

The mating connectors for the break-out boards are readily available from suppliers external to Agilent Technologies and are listed in Table 3-2 along with the connectors already mounted on the boards.

Table 3-2 Connector Part Numbers and Manufacturers

Connector Type	Break-out Board Output Connector Manufacturer Part Number	Mating Connector Manufacturer Part Number	Manufacturer
20-Pin	2520-6002UB	3421-6700 (wire connector)	3M
38-Pin Mictor	2-767004-2	767006-1 (board connector)	Tyco Electronics
40-Pin	2540-6002UB	3417-6700 (wire connector)	3M
68-Pin D-Subminiature	787170-7	749621-7 (wire connector)	Tyco Electronics
100-Pin Samtec	ASP-65067-01	ASP-65267-02 (wire connector)	Samtec

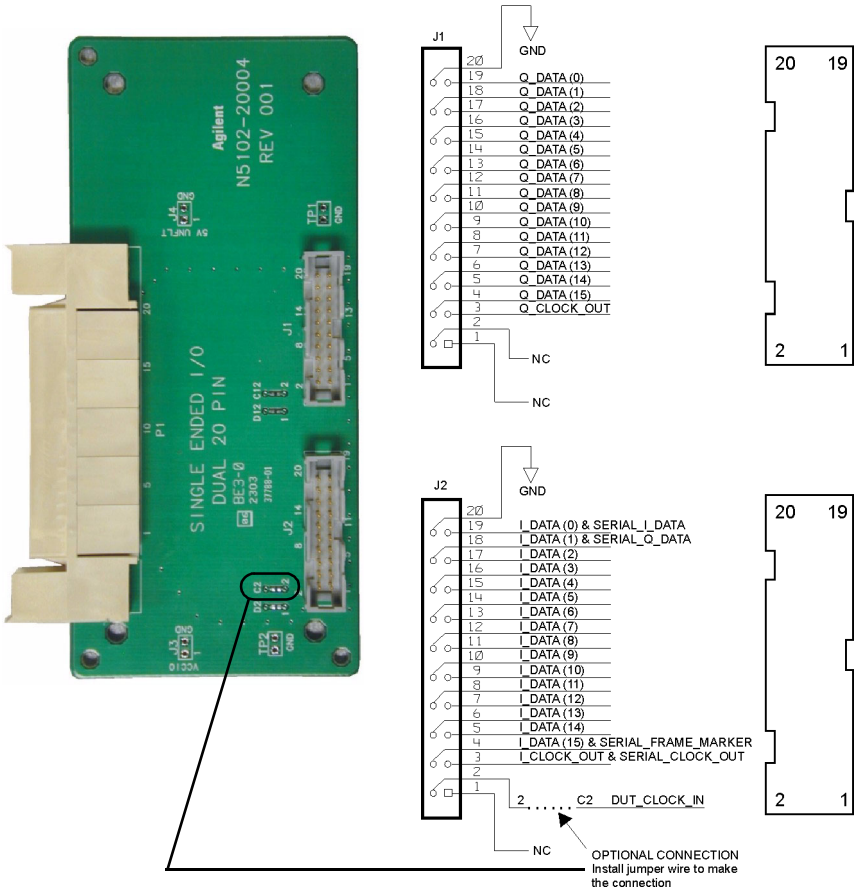
Dual 20-Pin Break-Out Board

Use this break-out board when single-ended testing is required and there are minimal connection points. It is most suitable at lower sample rates using easily constructed ribbon cables. Figure 3-1 shows this board along with the pin-out diagram for the connectors. The 20-pin connectors are a common 0.1 inch spaced header. Notice that the parallel I and Q signals are separated by connectors; J1 provides the Q signals and J2 provides the I signals. The serial signals are also provided on the J2 connector.

For the N5102A module to receive a clock through the Device Interface connector by way of this break-out board, a jumper wire is required at the 2 to C2 contacts. This is shown in Figure 3-1.

The VCCIO (selected high logic level voltage) is obtained at J3, while the + 5 volt unfiltered DC supply is acquired at J4.

Figure 3-1 Dual 20-Pin 0.1 Spaced Connector



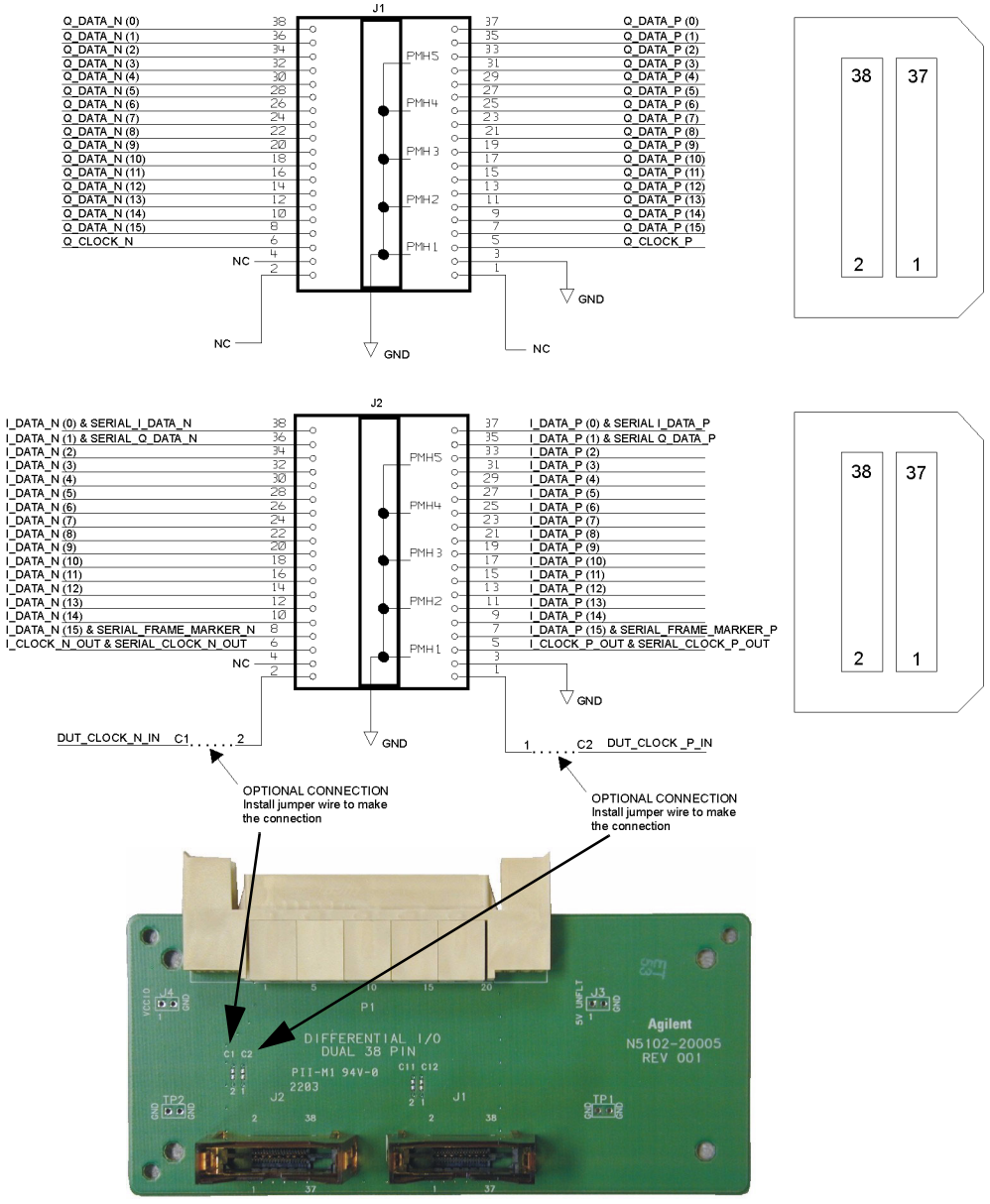
Dual 38-Pin Break-Out Board

This board is intended for differential testing, however it can also be used for single-ended signals. For single-ended signals, the data is transmitted on the positive lines. Figure 3-2 shows this break-out board along with the pin-out diagram for the connectors. Notice that the parallel I and Q signals are separated by connectors; J1 provides the Q signals and J2 provides the I signals. The serial signals are also provided on the J2 connector.

For the N5102A module to receive a clock through the Device Interface connector by way of this break-out board, a jumper wire is required at the 2 to C1 contacts for a negative clock and at the 1 to C2 contacts for a positive clock. This is shown in Figure 3-2.

The VCCIO (selected high logic level voltage) is obtained at J4, while the + 5 volt unfiltered DC supply is acquired at J3.

Figure 3-2 Dual 38-Pin Mictor Connector



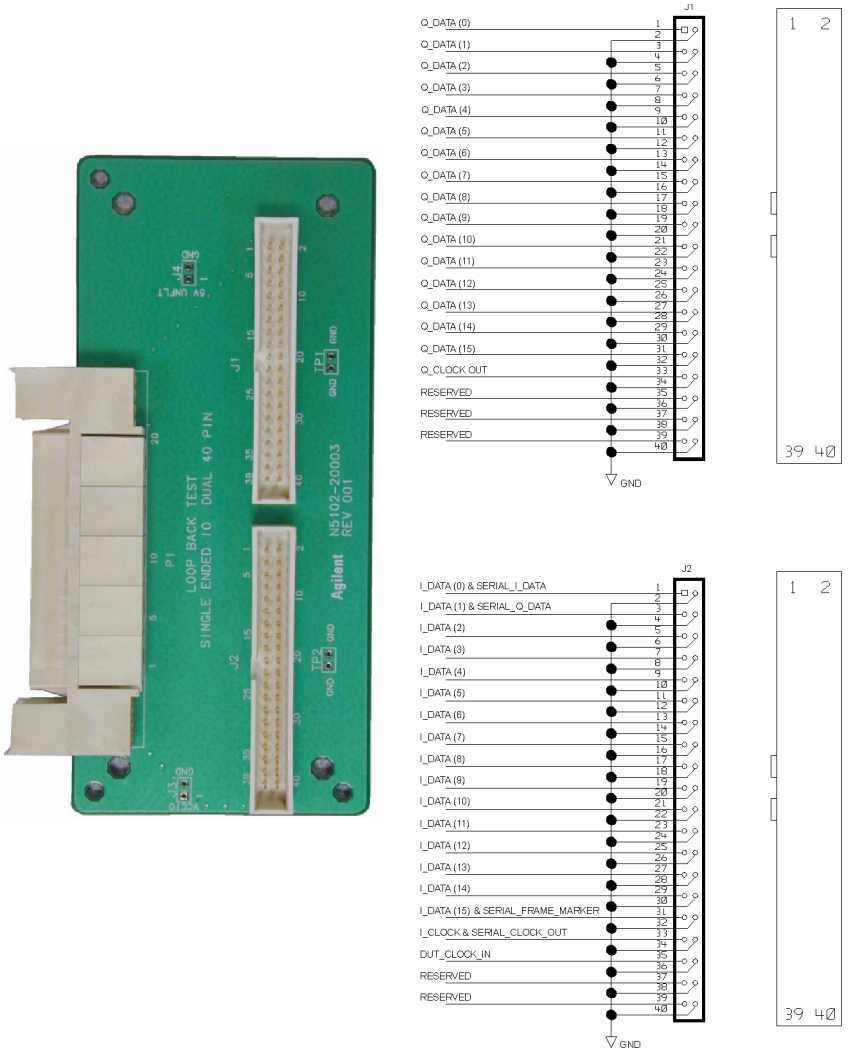
Dual 40 Pin Break-Out Board

This break-out board is useful for higher rate single-ended signals that benefit from a ground associated with each signal line. The 40-pin connectors are a common 0.1 inch spaced header. Figure 3-3 shows this break-out board along with the pin-out diagram for the connectors. Notice that the parallel I and Q signals are separated by connectors; J1 provides the Q signals and J2 provides the I signals. The serial signals are also provided on the J2 connector.

This board serves a dual function, one as a break-out board simplifying the connectivity of the device under test and the other as a loop back test board when performing N5102A module diagnostic tests.

The VCCIO (selected high logic level voltage) is obtained at J3, while the + 5 volt unfiltered DC supply is acquired at J4.

Figure 3-3 Dual 40 Pin 0.1 Spaced Header Connectors



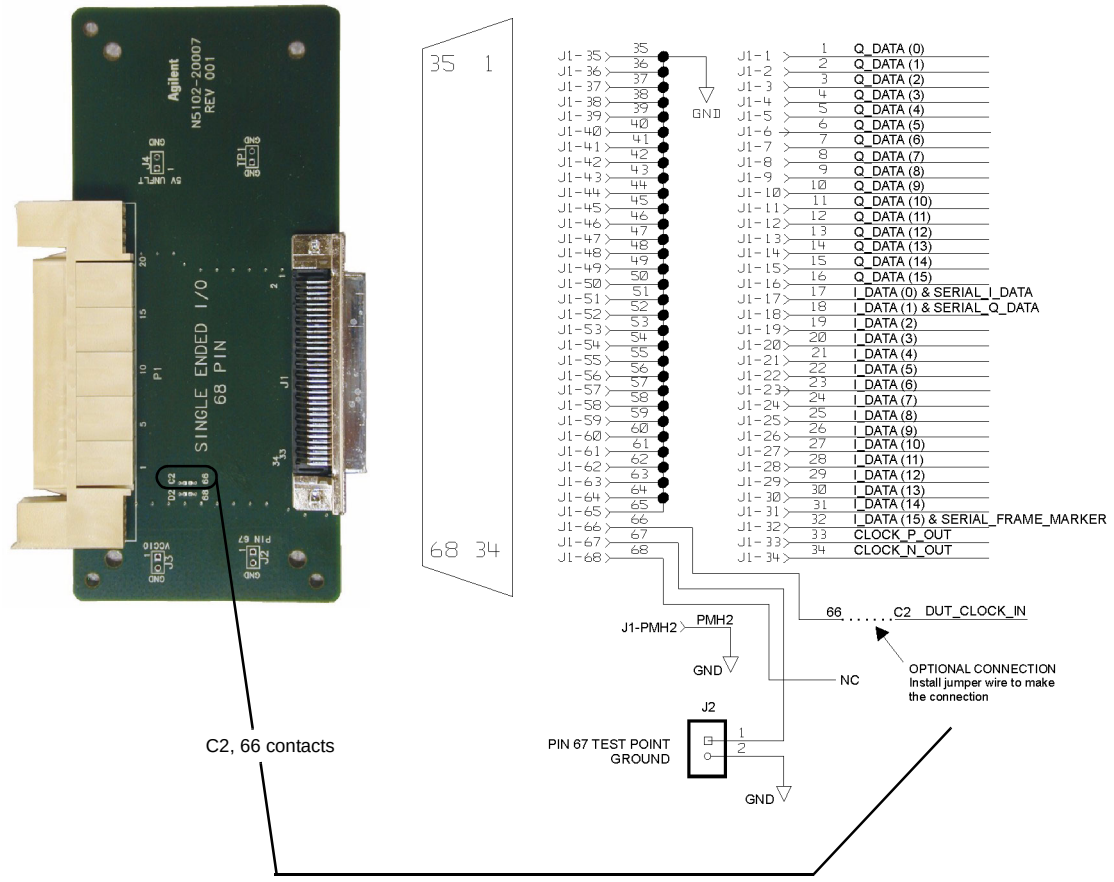
Single 68-Pin SCSI Style Break-Out Board

This break-out board is intended for single-ended testing. The connector is a SCSI style interface that is compatible with some existing products that provide a digital data output. The serial signals are transmitted on the I data lines. Figure 3-4 shows this break-out board along with the pin-out diagram for the output connector.

For the N5102A module to receive a clock through the Device Interface connector by way of this break-out board, a jumper wire is required at the 66 to C2 contacts. This is shown in Figure 3-4.

The VCCIO (selected high logic level voltage) is obtained at J3, while the + 5 volt unfiltered DC supply is acquired at J4.

Figure 3-4 Single 68-Pin D-Subminiature SCSI Style Connector

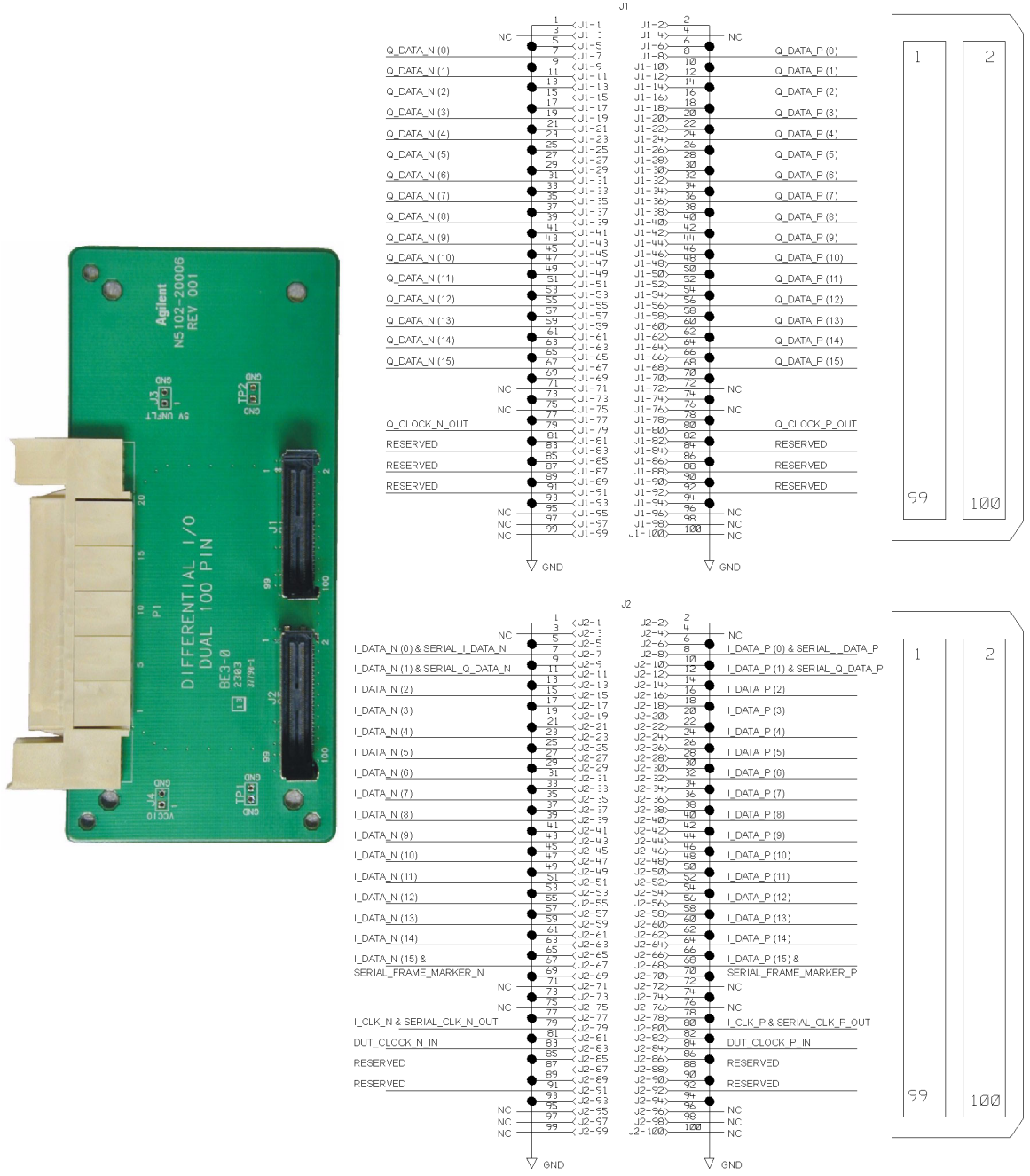


Dual 100-Pin Break-Out Board

This break-out board is intended for differential testing, however it can also be used for single-ended signals. For single-ended signals, the data is transmitted on the positive lines. Figure 3-5 shows this break-out board along with the pin-out diagram for the connectors. Notice that the parallel I and Q signals are separated by connectors; J1 provides the Q signals and J2 provides the I signals. Serial signals are also provided on the J2 connector.

The VCCIO (selected high logic level voltage) is obtained at J4, while the + 5 volt unfiltered DC supply is acquired at J3.

Figure 3-5 Dual 100-Pin Samtec Connector



Device Interface Connector

The figures and information shown in this section will assist when customizing a connection solution for the device under test using the device interface mating connector (see "Device Interface Mating Connector" on page 39). The signal contact layout for the Device Interface connector is shown in Figure 3-6 and the connector pin-out is shown in Figure 3-7 and Figure 3-8.

Figure 3-6 Device Interface Connector Layout

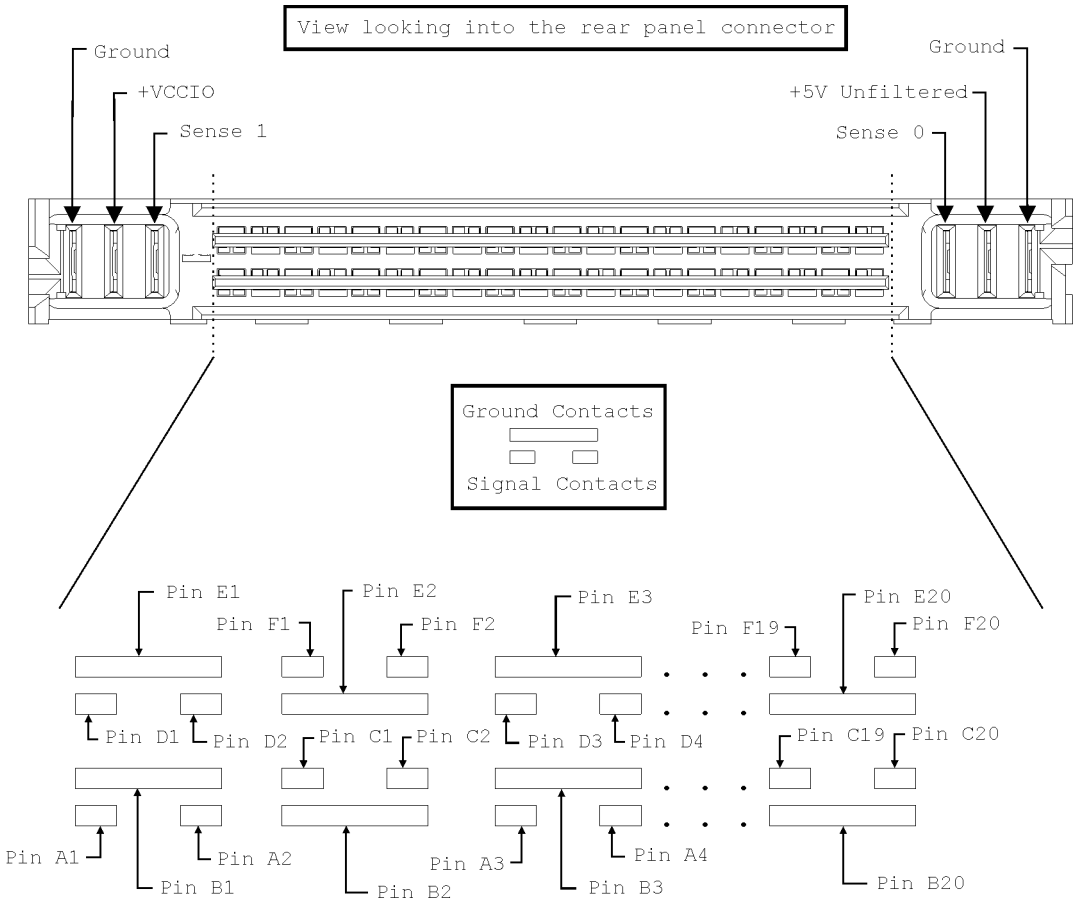


Figure 3-7 Device Interface Connector Pin-Out

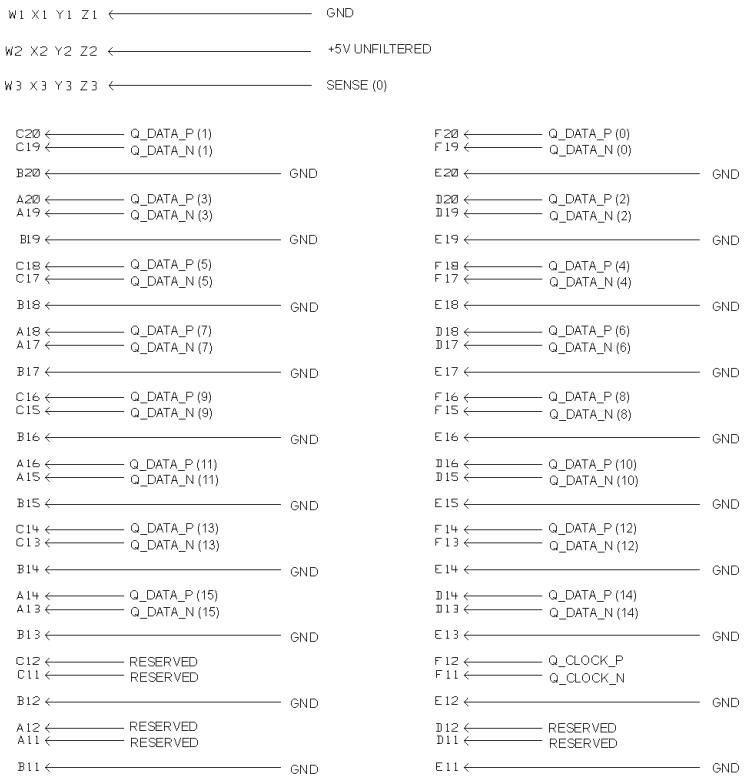
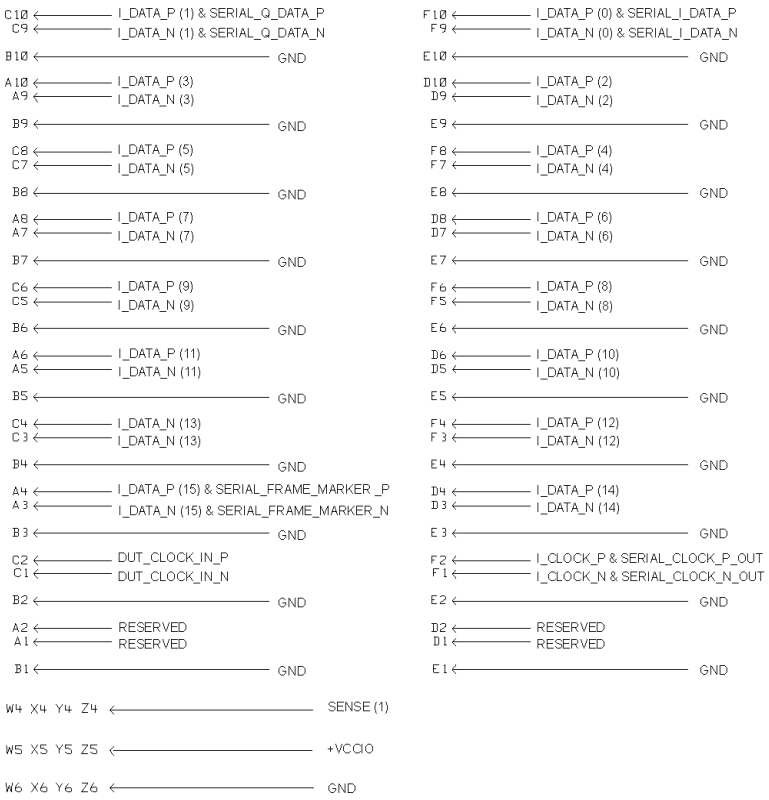


Figure 3-8 Device Interface Connector Pin-Out (continued)



Input and Output Clock Signals

There are multiple output clock lines and two input clock lines to handle differential clocking. The N5102A module can be configured to accept the device under test clock through the Device Interface connector for data clocking. Using the input clock signal from the Device Interface connector is an alternative to using a clock signal applied to the Clock In connector. Table 3-3 lists the Device Interface connector pins for the different clock signals and the serial frame marker.

Table 3-3 Clock Signal and Serial Frame Marker Lines

Clock Signal Type	Pin
Output Q-Clock Pos	F12
Output Q-Clock Neg	F11
Output I-Clock Pos	F2
Output I-Clock Neg	F1
Output Serial Clock Pos	F2
Output Serial Clock Neg	F1
Output Serial Frame Marker Pos	A4
Output Serial Frame Marker Neg	A3
Input Clock Signal (DUT Clock) Pos	C2
Input Clock Signal (DUT Clock) Neg	C1

Data Lines

There are 64 data lines on the Device Interface connector that allow for either differential or single-ended signals. These 64 data lines consist of 32-I lines (16 positive and 16 negative), and 32-Q lines (16 positive and 16 negative). Single-ended signals are routed on the positive data lines. Table 3-4 shows which data lines are used for a given signal.

Table 3-4 Data Lines

Signal	Serial Data		Parallel Data[1]	
	I	Q	I	Q
Differential	Positive and negative lines: F9 & F10	Positive and negative lines: C9 & C10	Positive and negative lines 0–16 (A3–A10, C3–C10 D3–D10, F3–F10)	Positive and negative lines 0–16 (A13–A20, C13–C20, D13–D20, F13–F20)
Single-Ended	F10	C10	Positive lines 0–16 (A4, A6, A8, A10, C4, C6, C8, C10, D4, D6, D8, D10, F4, F6, F8, F10)	Positive lines 0–16 (A14, A16, A18, A20, C14, C16, C18, C20, D14, D16, D18, D20, F14, F16, F18, F20)

1. Parallel interleaving (IQ and QI) occurs on the I data lines.

DC Supply

Referring to Figure 3-6, notice that the interface module provides an unfiltered +5 volts DC supply through the Device Interface connector. This DC supply provides up to 100 mA and has a self-resettable fuse. Use this DC current to bias components on the device under test where the noise will not compromise test results.

VCCIO

The Device Interface connector also provides a connection for the VCCIO that can be measured at a test point on each break-out board. The VCCIO amplitude is equal to the high voltage level of the selected logic type.

Device Interface Mating Connector

A mating connector for the Device Interface port is supplied to make the device under test connection easier when none of the break-out boards offer a connection solution for the device.

There are two ways to use the mating connector. One is to attach wires directly to the pins providing a quick connection solution. The other is to make a PC board with a footprint that matches the connector mounting pins. Figure 3-9 shows the layout of the signal contacts while looking directly into the connector and the pin footprint while viewing the connector from the bottom. Figure 3-10 shows the connector footprint for a PC board.

The signal pin-out for the connector can be obtained from Figure 3-7 on page 35 and Figure 3-8 on page 36. These figures display the pin-out diagrams for the N5102A module Device Interface connector.

Table 3-5 provides the manufacturer and the part numbers for the Device Interface connector and its mate. Both connectors are available from suppliers external to Agilent Technologies.

Table 3-5

Connector Type	Connector Manufacturer Part Number	Mating Connector Manufacturer Part Number	Manufacturer
144-Pin Z-Dok+	1367550-5	1367555-2 (board connector)	Tyco Electronics

Figure 3-9 Z-Dok+ Device Interface Mating Connector Layout and Footprint

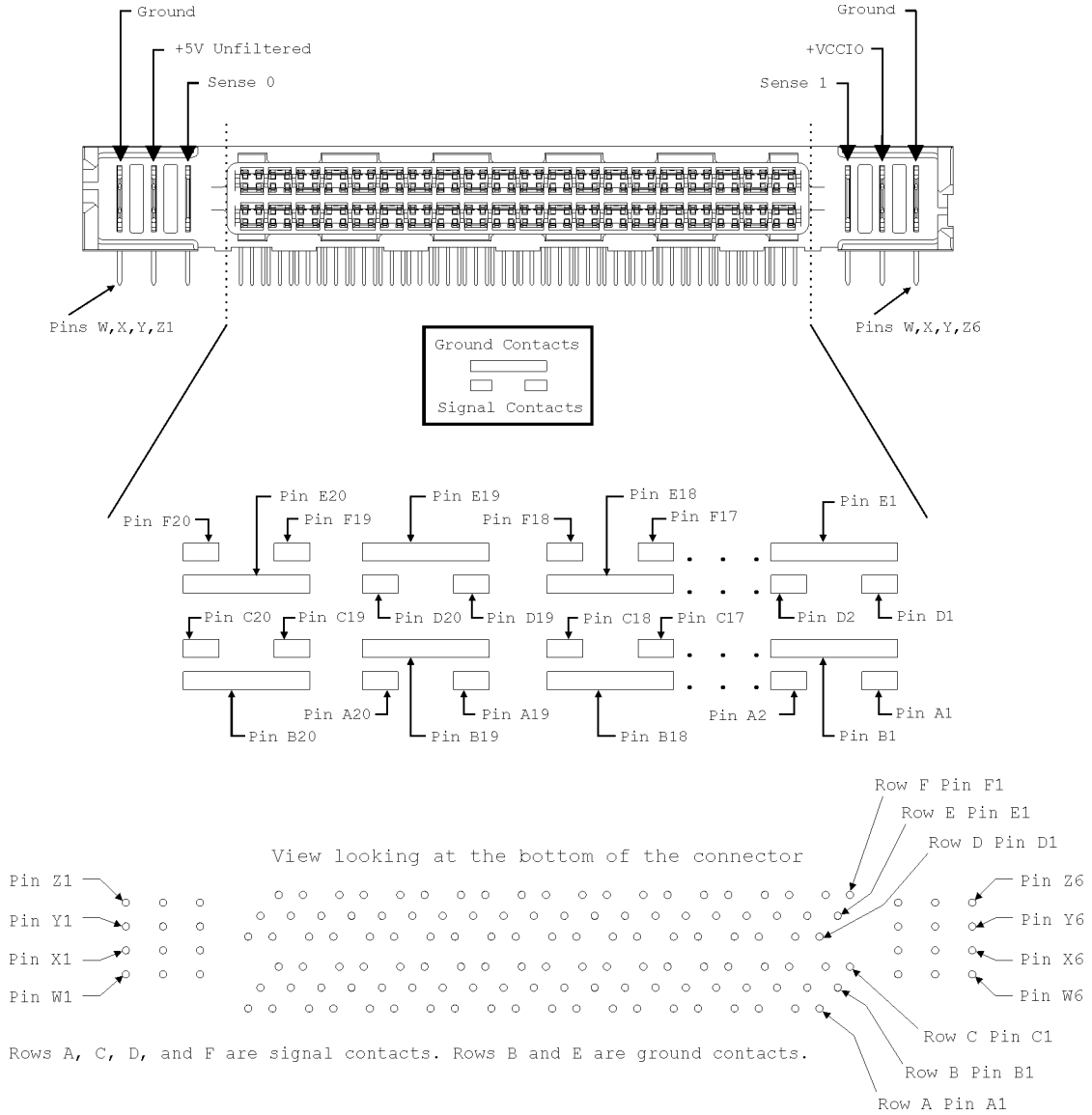
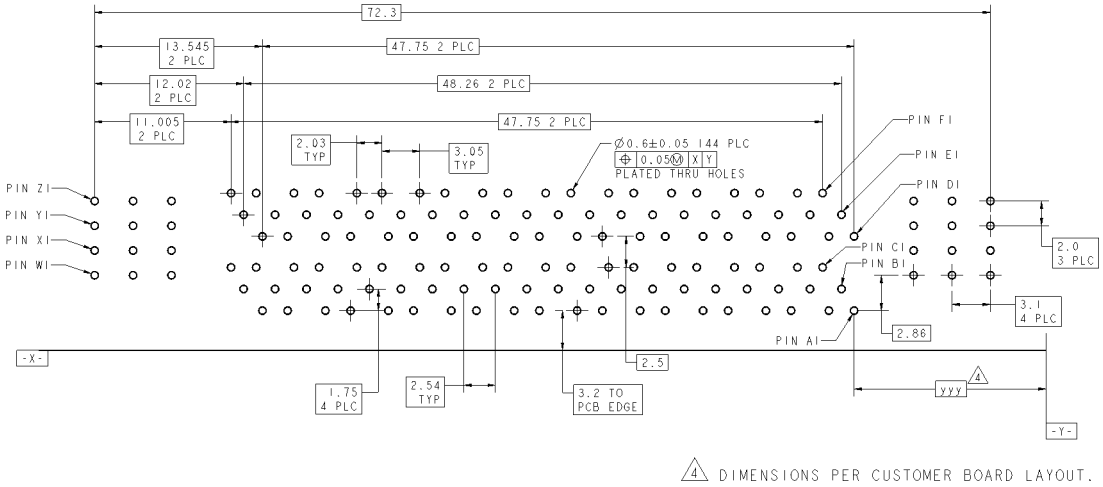


Figure 3-10 Z-Dok+ Device Interface Mating Connector PC Board Foot Print

Component Side Shown

It is recommended that you check the Tyco Electronics web site for the most current PC board footprint drawing.

Rows A, C, D, and F are signal contacts. Rows B and E are ground contacts.



4 Operation

This chapter provides clock timing information for the N5102A Baseband Studio digital signal interface module, and procedures for configuring the digital signal parameters.

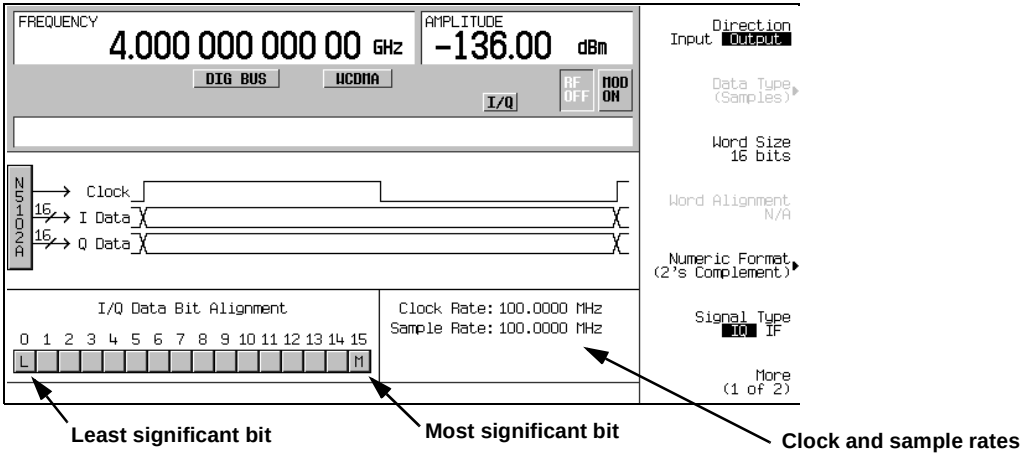
Clock Timing

This section describes how clocking for the digital data is provided. Clock timing information and diagrams are supplied for the different port configurations (serial, parallel, or parallel interleaved data transmission) and phase and skew settings. All settings for the interface module are available on the signal generator user interface (UI).

Clock and Sample Rates

A sample is a group of bits where the size of the sample is set using the **Word Size** softkey. The clock is the signal that tells when the bits of a sample are valid (in a non-transition state). The clock and sample rates are displayed in the first-level and data setup softkey menus. The clock rate and sample rate are usually the same. They will differ when serial mode is selected, or when there are multiple clocks per sample.

Figure 4-1 Data Setup Menu for a Parallel Port Configuration



Refer to "Bit Order MSB LSB" on page 88.

The N5102A module clock rate is set using the **Clock Rate** softkey and has a range of 1 kHz to 400 MHz. The sample rate is automatically calculated and has a range of 1 kHz to 100 MHz. These ranges can be smaller depending on logic type, data parameters, and clock configuration.

Maximum Clock Rates

The N5102A module maximum clock rate is dependent on the logic and signal type. Table 4-1 and Table 4-2 show the warranted rates and the maximum clock rates for the various logic and signal types.

Notice that LVDS in the output mode using an IF signal is the only logic type where the warranted and maximum rates are the same.

Table 4-1 Warranted Parallel Output Level Clock Rates and Maximum Clock Rates

Logic Type	Warranted Level Clock Rates		Maximum Clock Rates (typical)	
	IQ Signal Type	IF Signal Type[1]	IQ Signal Type	IF Signal Type
LVTTL and CMOS	100 MHz	100 MHz	150 MHz	150 MHz
LVDS	200 MHz	400 MHz	400 MHz	400 MHz

1. The IF signal type is not available for a serial port configuration.

Table 4-2 Warranted Parallel Input Level Clock Rates and Maximum Clock Rates

Logic Type	Warranted Level Clock Rates	Maximum Clock Rates (typical)
LVTTL and CMOS	100 MHz	100 MHz
LVDS	100 MHz	400 MHz

The levels will degrade above the warranted level clock rates, but they may still be usable.

Serial Port Configuration Clock Rates

For a serial port configuration, the lower clock rate limit is determined by the word size (word size and sample size are synonymous), while the maximum clock rate limit remains constant at 150 MHz for LVTTL and CMOS logic types, and 400 MHz for an LVDS logic type.

The reverse is true for the sample rate. The lower sample (word) rate value of 1 kHz remains while the upper limit of the sample rate varies with the word size. For example, a five-bit sample for an LVTTL or CMOS logic type yields the following values in serial mode:

- Clock rate of 5 kHz through 150 MHz
- Sample rate of 1 kHz through 30 MHz

Refer to Table 4-3 and Table 4-4, for the serial clock rates.

Table 4-3 Output Serial Clock Rates

Logic Type	Minimum Rate	Maximum Rate
LVDS	1 x (word size) kHz	400 MHz

Table 4-3 Output Serial Clock Rates

Logic Type	Minimum Rate	Maximum Rate
LVTTL and CMOS	1 x (word size) kHz	150 MHz

Table 4-4 Input Serial Clock Rates

Logic Type	Data Type	Minimum Rate	Maximum Rate
LVDS	Samples	1 x (word size) kHz	400
	Pre-FIR Samples	1 x (word size) kHz	the smaller of: 50[1] x (word size) MHz or 400 MHz
LVTTL and CMOS	N/A	1 x (word size) kHz	150 MHz

1. The maximum sample rate depends on the selected filter when the data rate is Pre-FIR Samples. Refer to "Input Mode" on page 58 for more information.

Parallel and Parallel Interleaved Port Configuration Clock Rates

Parallel and parallel interleaved port configurations have other limiting factors for the clock and sample rates:

- logic type
- Clocks per sample selection
- IQ or IF digital signal type

Clocks per sample (clocks/sample) is the ratio of the clock to sample rate. For an IQ signal type, the sample rate is reduced by the clocks per sample value when the value is greater than one. For an IF signal or an input signal, clocks per sample is always set to one. Refer to Table 4-5 for the Output mode parallel and parallel interleaved port configuration clock rates.

Table 4-5 Output Parallel and Parallel Interleaved Clock Rates

Logic Type	Signal Type	Minimum Rate	Maximum Rate
LVDS	IQ	1 x (clocks/sample) kHz	the smaller of: 100 x (clocks /sample) MHz or 400 MHz
	IF	4 kHz	400 MHz
Other	IQ	1 x (clocks/sample) kHz	the smaller of: 100 x (clocks /sample) MHz or 150 MHz
	IF	4 kHz	150 MHz

For Input mode, the maximum clock rate is limited by the following factors:

- sample size
- data type
- selected filter for Pre-FIR Samples

Refer to Table 4-6 for the Input mode parallel and parallel interleaved port configuration clock rates.

Table 4-6 Input Parallel and Parallel Interleaved Clock Rates

Logic Type	Data Type	Minimum Rate	Maximum Rate
N/A	Samples	1 kHz	100 MHz
	Pre-FIR Samples	1 kHz	50[1] MHz

1. The maximum sample rate depends on the selected filter when the data rate is Pre-FIR Samples. Refer to "Input Mode" on page 58 for more information.

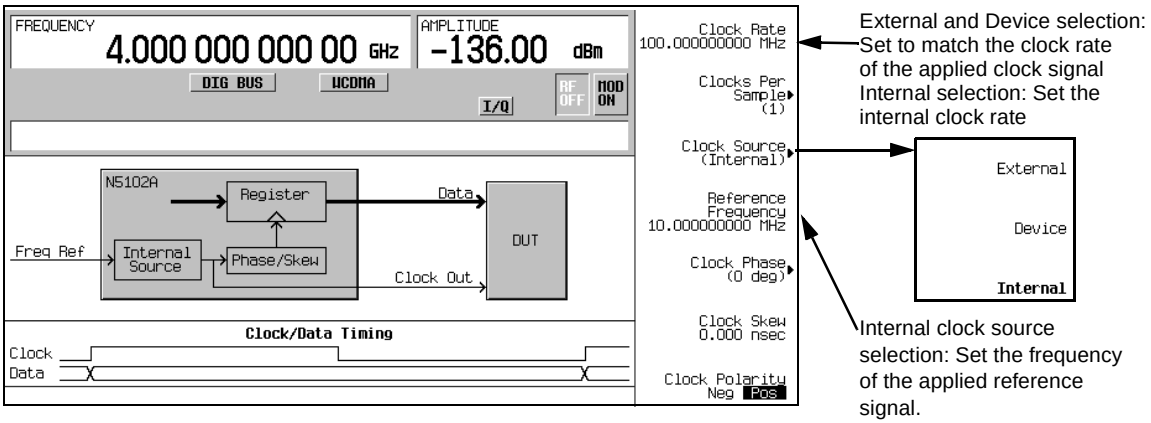
Clock Source

The clock signal for the N5102A module is provided in one of three ways through the following selections:

- Internal: generated internally in the interface module (requires an external reference)
- External: generated externally through the Ext Clock In connector
- Device: generated externally through the Device Interface connector

The clock source is selected using the N5102A module UI on the signal generator, see Figure 4-2.

Figure 4-2 Clock Source Selection



When you select a clock source, you must let the N5102A module know the frequency of the clock signal using the **Clock Rate** softkey. In the internal clock source mode, use this softkey to set the internal clock rate. For device and external clock sources, this softkey must reflect the frequency of the applied clock signal.

When the clock source is Internal, a frequency reference must be applied to the Freq Ref connector. The frequency of this applied signal needs to be specified using the **Reference Frequency** softkey, unless the current setting matches that of the applied signal.

The selected clock source provides the interface module output clock signal at the Clock Out and the Device Interface connectors.

Common Frequency Reference

The clocking flexibility of the digital signal interface module allows the setting of arbitrary clock rates for the device under test. In general, the clock rate inside the ESG/PSG will be different from the interface module clock rate, so the interface module performs a rate conversion. An important aspect of this conversion is to have accurate clock rate information to avoid losing data. The module relies on relative clock accuracy, instead of absolute accuracy, that must be ensured by using a single frequency reference for all clock rates involved in the test setup. This can be implemented in various ways (see the five drawings in Figure 4-3 on page 50), but whatever way it is implemented, the clock inside the signal generator must have the same base frequency reference as the clock used by the device under test.

ESG/PSG Frequency Reference Connections

When a frequency reference is connected to the signal generator, it is applied to one of two rear panel connectors:

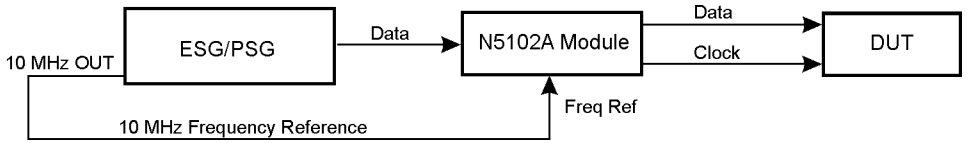
- 10 MHz IN
- BASEBAND GEN REF IN

The BASEBAND GEN REF IN connector will accept a frequency reference in the range of 1 to 100 MHz. If the external or device under test clock source cannot provide or accept a frequency reference, that clock signal can be applied to this connector and used as the frequency reference (as long as the frequencies are within the specified range).

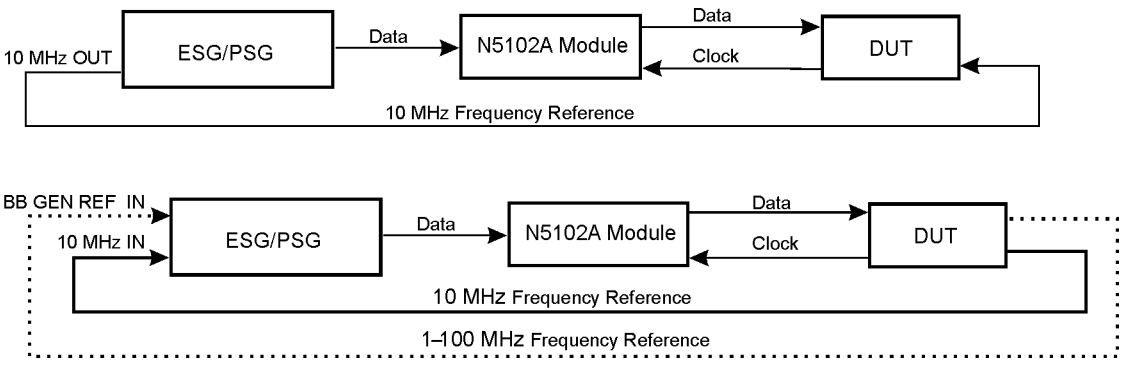
Whenever an external clock signal or frequency reference is connected to the BASEBAND GEN REF IN connector, its frequency needs to be entered into the current signal generator modulation format. For information on the BASEBAND GEN REF IN connector for the ESG, refer to the *Agilent ESG Vector Signal Generator User's Guide*, and for the PSG, refer to the *Agilent PSG Signal Generators User's Guide*. For information on the associated softkeys and fields for entering the frequency of the applied clock signal or frequency reference, refer to the *Agilent ESG Vector Signal Generator Key and Data Field Reference* or the *Agilent PSG Signal Generators Key Reference*.

Figure 4-3 Frequency Reference Setup Diagrams for the N5102A Module Clock Signal

Internally Generated Clock

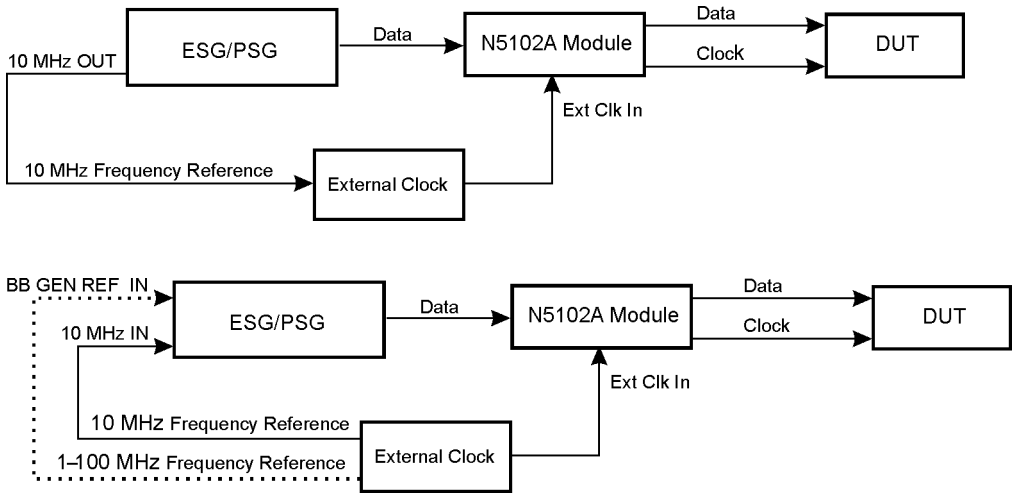


Device (DUT) Supplied Clock



NOTE: Use only one of the two signal generator frequency reference inputs.

Externally Supplied Clock

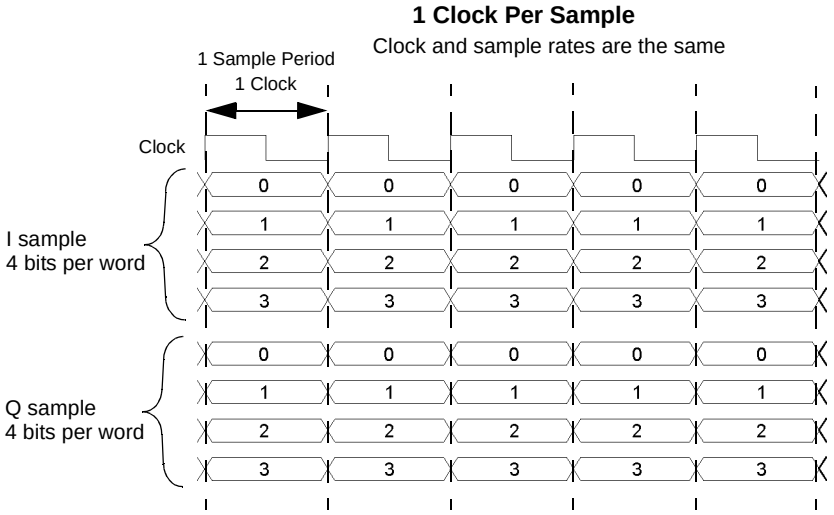


NOTE: Use only one of the two signal generator frequency reference inputs.

Clock Timing for Parallel Data

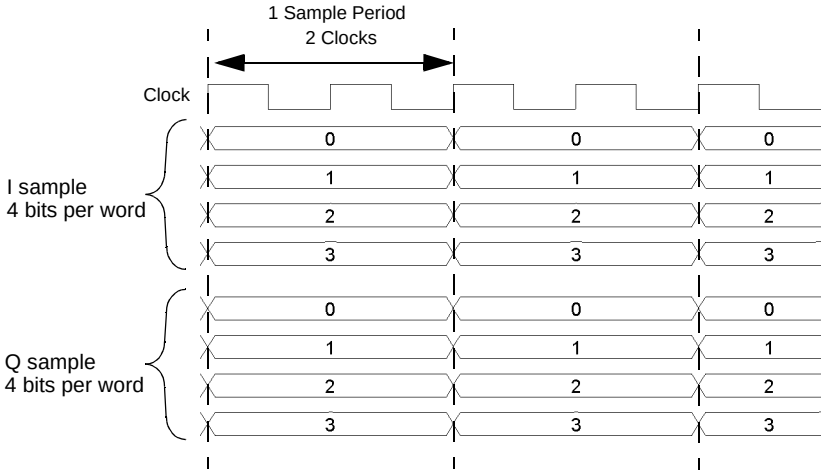
Some components require multiple clocks during a single sample period. (A sample period consists of an I and Q sample). For parallel data transmissions, you can select one, two, or four clocks per sample. For clocks per sample greater than one, the I and Q samples are held constant to accommodate the additional clock periods. This reduces the sample rate relative to the clock rate by a factor equal to the clocks per sample selection. For example, when four is selected, the sample rate is reduced by a factor of four (sample rate to clock rate ratio). Figure 4-4 demonstrates the clock timing for each clocks per sample selection. For input mode, the clocks per sample setting is always one.

Figure 4-4 Clock Sample Timing for Parallel Port Configuration



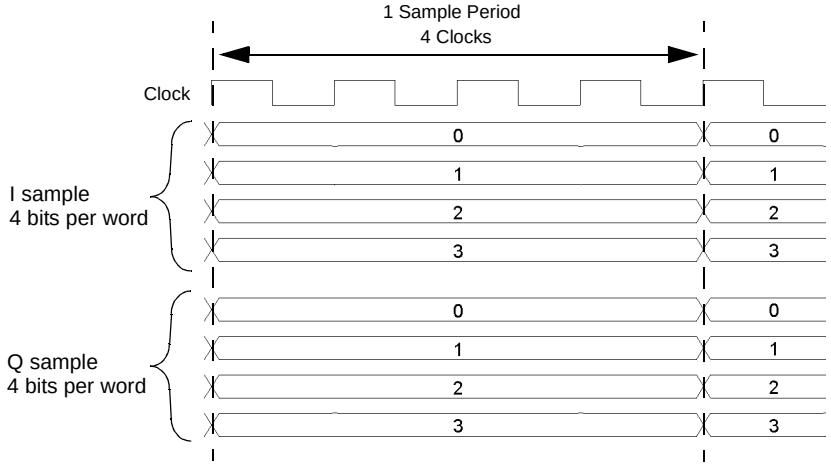
2 Clocks Per Sample

Sample rate decreases by a factor of two



4 Clocks Per Sample

Sample rate decreases by a factor of four



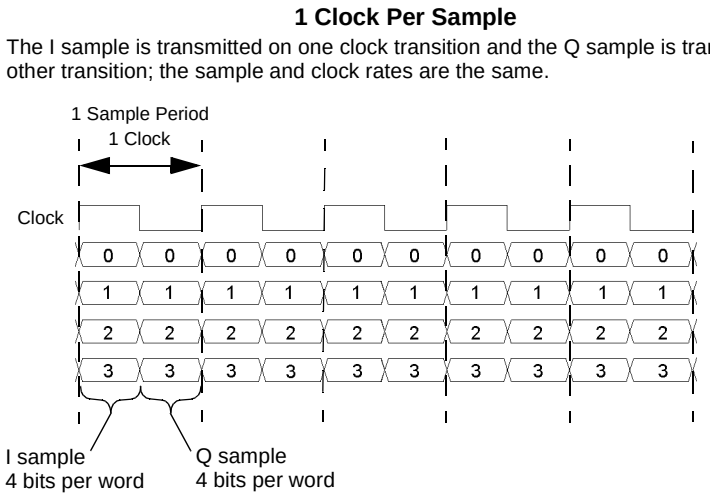
Clock Timing for Parallel Interleaved Data

The N5102A module provides the capability to interleave the digital I and Q samples. There are two choices for interleaving:

- IQ, where the I sample is transmitted first
- QI, where the Q sample is transmitted first

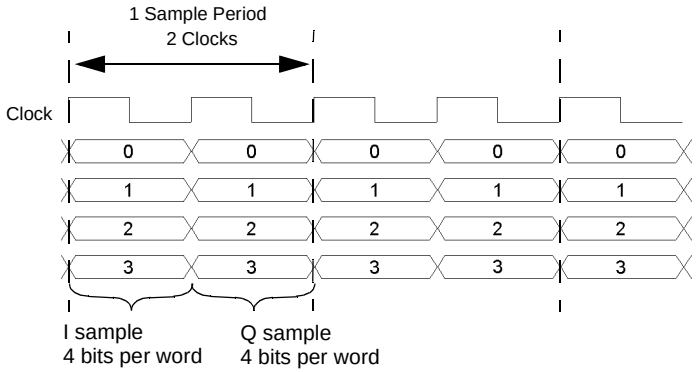
When parallel interleaved is selected, all samples are transmitted on the I data lines. This effectively transmits the same number of samples during a sample period on half the number of data lines as compared to non-interleaved samples. (A sample period consists of an I and Q sample.) Clocks per sample is still a valid parameter for parallel interleaved transmissions and creates a reduction in the sample rate relative to the clock rate. The clocks per sample selection is the ratio of the reduction. Figure 4-5 shows each of the clocks per sample selections, for a parallel IQ interleaved port configuration , using a word sized of four bits and the clock timing relative to the I and Q samples. For a parallel QI interleaved port configuration, just reverse the I and Q sample positions. For input mode, the clocks per sample setting is always one.

Figure 4-5 Clock Timing for a Parallel IQ Interleaved Port Configuration



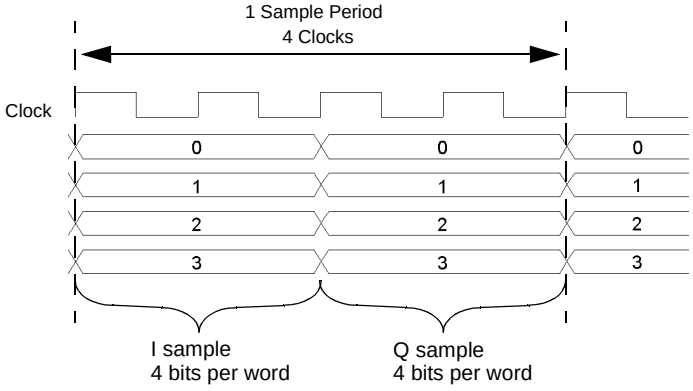
2 Clocks Per Sample

The I sample is transmitted for one clock period and the Q sample is transmitted during the second clock period; the sample rate decreases by a factor of two.



4 Clocks Per Sample

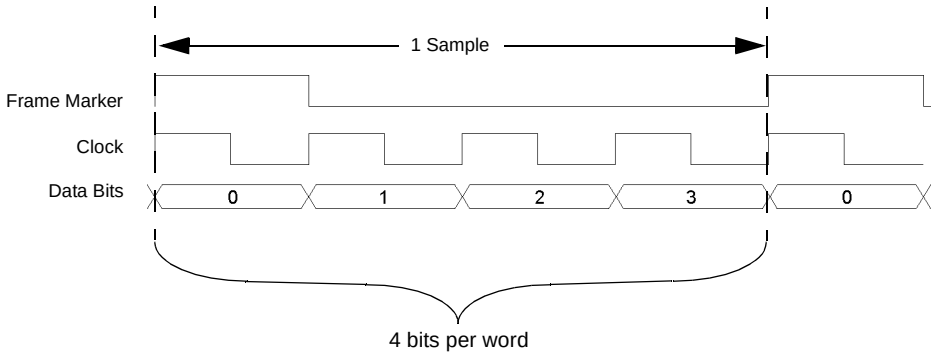
The I sample is transmitted for the first two clock periods and the Q sample is transmitted during the second two clock periods; the sample rate is decreased by a factor of four.



Clock Timing for Serial Data

Figure 4-6 shows the clock timing for a serial port configuration. Notice that the serial transmission includes frame pulses that mark the beginning of each sample where the clock delineates the beginning of each bit. For serial transmission, the clock and the bit rates are the same, but the sample rate varies depending on the number of bits per word that are entered using the **Word Size** softkey. The number of bits per word is the same as the number of bits per sample.

Figure 4-6 Clock Timing for a Serial Port Configuration



Clock Timing for Phase and Skew Adjustments

The N5102A module provides phase and skew adjustments for the clock relative to the data and can be used to align the clock with the valid portion of the data. The phase has a 90 degree resolution (0, 90, 180, and 270 degree selections) for clock rates from 10 to 200 MHz and a 180 degree resolution (0 and 180 degree selections) for clock rates below 10 MHz and greater than 200 MHz.

The skew is displayed in nanoseconds with a maximum range of ±5 ns using a maximum of ±127 discrete steps. Both the skew range and the number of discrete steps are variable with a dependency on the clock rate. The skew range decreases as the clock rate is increased and increases as the clock rate is decreased. The maximum skew range is reached at a clock rate of approximately 99 MHz and is maintained down to a clock rate of 25 MHz. For clock rates below 25 MHz, the skew adjustment is unavailable.

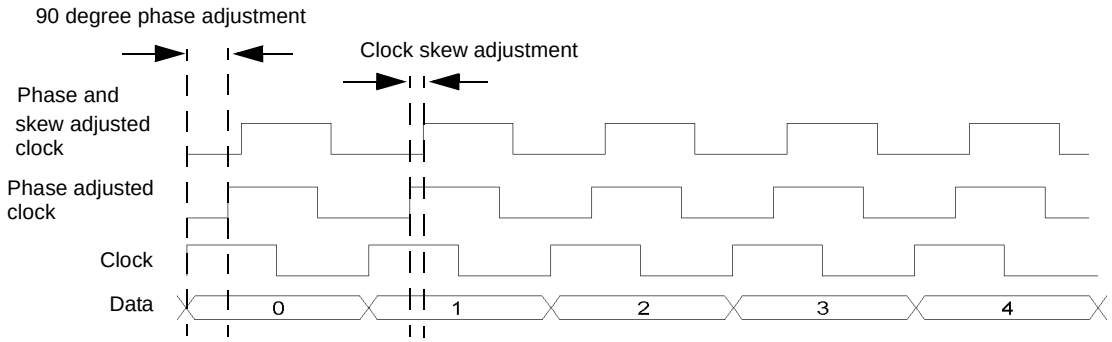
A discrete step is calculated using the following formula:

$$\frac{1}{256 \times \text{Clock Rate}}$$

The number of discrete steps required to reach the maximum skew range decreases at lower frequencies. For example, at a clock rate of 50 MHz, 127 steps would exceed the maximum skew range of ±5 ns, so the actual number of discrete steps would be less than 127.

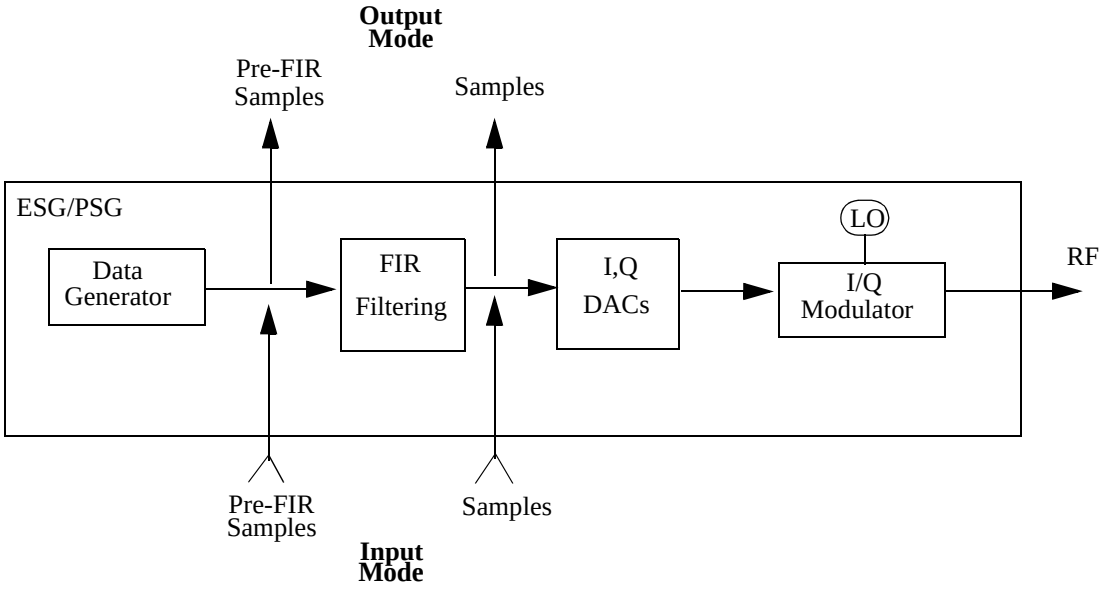
Figure 4-7 is an example of a phase and skew adjustment and shows the original clock and its phase position relative to the data after each adjustment. Notice that the skew adjustment adds to the phase setting.

Figure 4-7 Clock Phase and Skew Adjustments



Data Types

The following block diagram indicates where in the ESG/PSG signal generation process the data is injected for input mode or tapped for output mode.



Output Mode

When using an ARB format, the data type is always Samples and no filtering is applied to the data samples.The samples are sent to the digital module at the ARB sample clock rate.

For real-time formats, choosing Samples as the data type will send filtered samples to the digital module at a rate between 50 MHz and 100 MHz. Selecting Pre-FIR Samples, sends unfiltered samples to the digital module at a rate equal to the sample rate of the current format.

Input Mode

When the data type is Samples, the data samples coming through the digital module are injected at a point that bypasses the filtering process.

If Pre-FIR Samples is selected, the data samples are injected before the filtering process. The maximum rate will be determined by the selected filter. Refer to Table 4-7.

Table 4-7 Maximum Sample Rate for Selected Filter

Filter	Maximum Rate
Gaussian Nyquist Root Nyquist Rectangle Edge UN3/4 GSM Gaussian IS-95 IS 95 w/EQ	50 MHz
IS-95 Mod IS-95 Mod w/EQ	25 MHz
APCO 25 C4FM	12.5 MHz

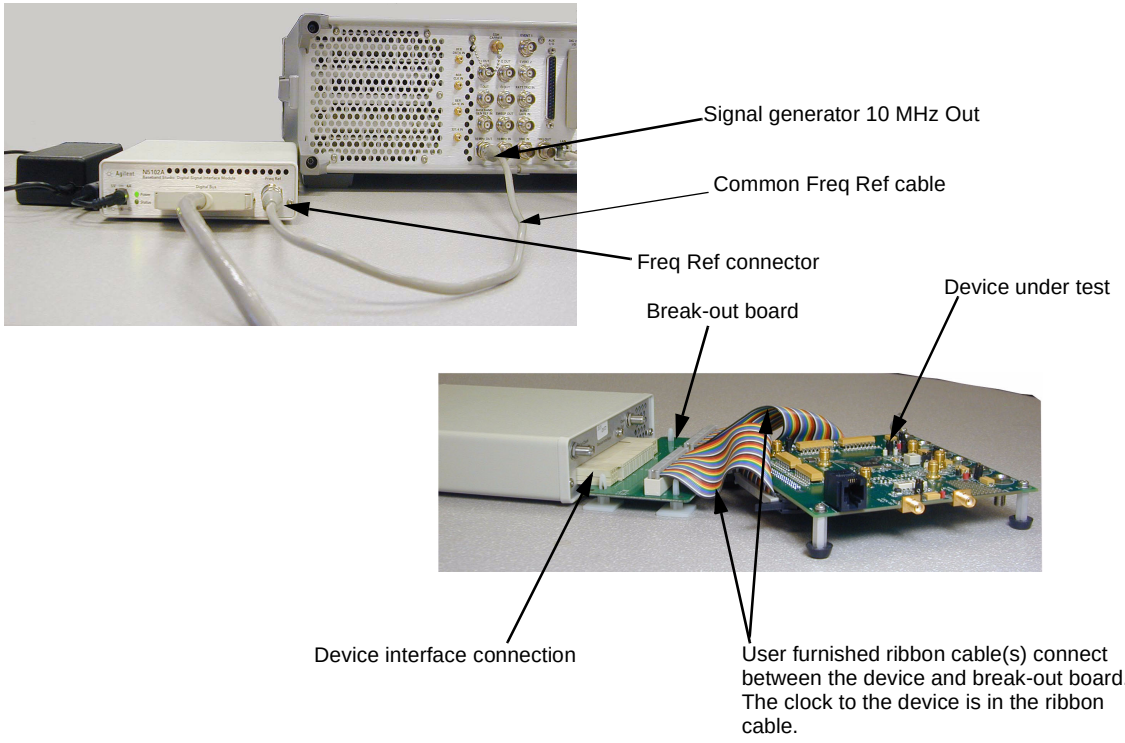
The **Filter** softkey accesses a menu that enables you set the desired filtering parameters.

Connecting the Clock Source and the Device Under Test

As shown in Figure 4-3 on page 50, there are numerous ways to provide a common frequency reference to the system components (ESG/PSG, N5102A module, and the device under test). Figure 4-8 shows an example setup where the signal generator supplies the common frequency reference and the N5102A module is providing the clock to the device.

CAUTION The Device Interface connector on the interface module communicates using high speed digital data. Use ESD precautions to eliminate potential damage when making connections.

Figure 4-8 Example Setup using the ESG/PSG 10 MHz Frequency Reference



NOTE You must disconnect the digital bus cable and the digital module while downloading firmware to the ESG/PGSG.

1. Refer to the five setup diagrams in Figure 4-3 on page 50 and connect the frequency reference cable according to the clock source.
2. If an external clock source is used, connect the external clock signal to the Ext Clock In connector on the interface module.
3. Select the break-out board that has the output connector suited for the application.

NOTE If the Device Interface mating connector is used with the device under test, refer to Figure 4-8 for the device interface connection and connect the device to the N5102A module. Then proceed to "Operating the N5102A Module in Output Mode" on page 62 or "Operating the N5102A Module in Input Mode" on page 71.

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4. Refer to Figure 4-8. Connect the break-out board to the Device Interface connector on the N5102A module.
5. Connect the device to the break-out board.

Operating the N5102A Module in Output Mode

This section shows how to set the parameters for the N5102A module using the signal generator UI in the output direction. Each procedure contains a figure that shows the softkey menu structure for the interface module function being performed.

Setting up the Signal Generator Baseband Data

The digital signal interface module receives data from a baseband source and outputs a digital IQ or digital IF signal relative to the selected logic type. Because an ESG/PSG provides the baseband data, the first procedure in operating the interface module is configuring the ESG/PSG using one of the real-time or ARB modulation formats, or playing back a stored file using the Dual ARB player. For information on configuring the ESG, refer to the *Agilent ESG Vector Signal Generator User's Guide*, and for configuring the PSG, refer to the *Agilent PSG Signal Generators User's Guide*.

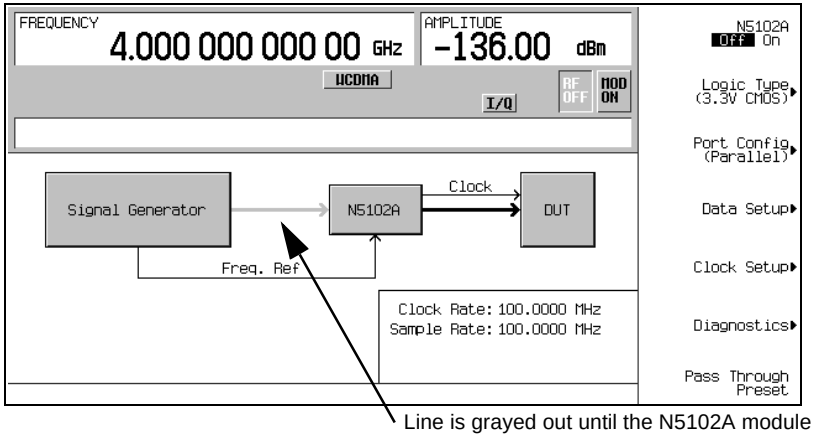
1. Preset the signal generator.
2. Select the modulation format (TDMA, Custom, and so forth) and set the desired parameters.
3. Turn-on the modulation format.

Accessing the N5102A Module User Interface

Press **Aux Fctn** > **N5102A Interface**.

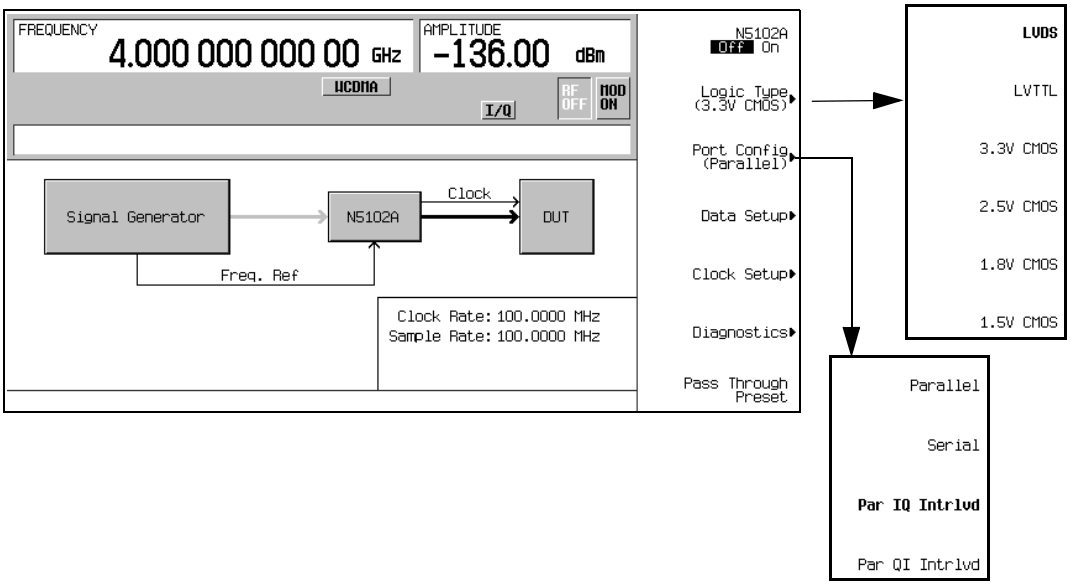
This accesses the UI (first-level softkey menu shown in Figure 4-9) that is used to configure the digital signal interface module. Notice the graphic, in the ESG/PSG display, showing a setup where the N5102A module is generating its own internal clock signal. This graphic changes to reflect the current clock source selection.

Figure 4-9 First-Level Softkey Menu



Choosing the Logic Type and Port Configuration

Figure 4-10 Logic and Port Configuration Softkey Menus



1. Refer to Figure 4-10. Press the **Logic Type** softkey.

   From this menu, choose a logic type.

CAUTION Changing the logic type can increase or decrease the signal voltage level going to the device under test. To avoid damaging the device and/or the N5102A module, ensure that both are capable of handling the voltage change.

2. Select the logic type required for the device being tested.

   A caution message is displayed whenever a change is made to the logic types, and a softkey selection appears requesting confirmation.

3. Refer to Figure 4-10. Press the **Port Configuration** softkey.

   In this menu, select either a serial, parallel, or parallel interleaved data transmission.

NOTE Within the data and clock setup softkey menus, some softkeys function relative to the current configuration. Softkeys that are grayed out are not available for the current setup. Refer to the help text to determine which parameter is causing the softkey to be unavailable. Press the **Help** hardkey on the ESG/PSG front panel and then the softkey that is unavailable.

4. Select the port configuration for the device.

Selecting the Output Direction

Press **Data Setup** > **Direction Input Output** to Output and press **Return**.

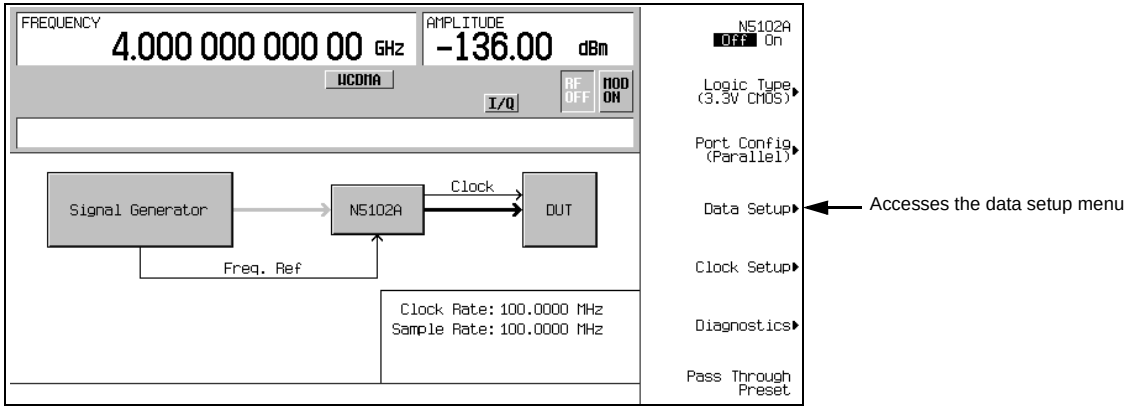
NOTE If Option 003 is the only option installed, the direction softkey will be unavailable and the mode will always be output. With both Option 003 (output mode) and Option 004 (input mode) installed, the default direction is output.

Selecting the Data Parameters

This procedure guides you through the data setup menu. Softkeys that have self-explanatory names are generally not mentioned. For example, the **Word Size** softkey. For more information on all of the softkeys, refer to "Softkey and SCPI Command Descriptions" on page 84.

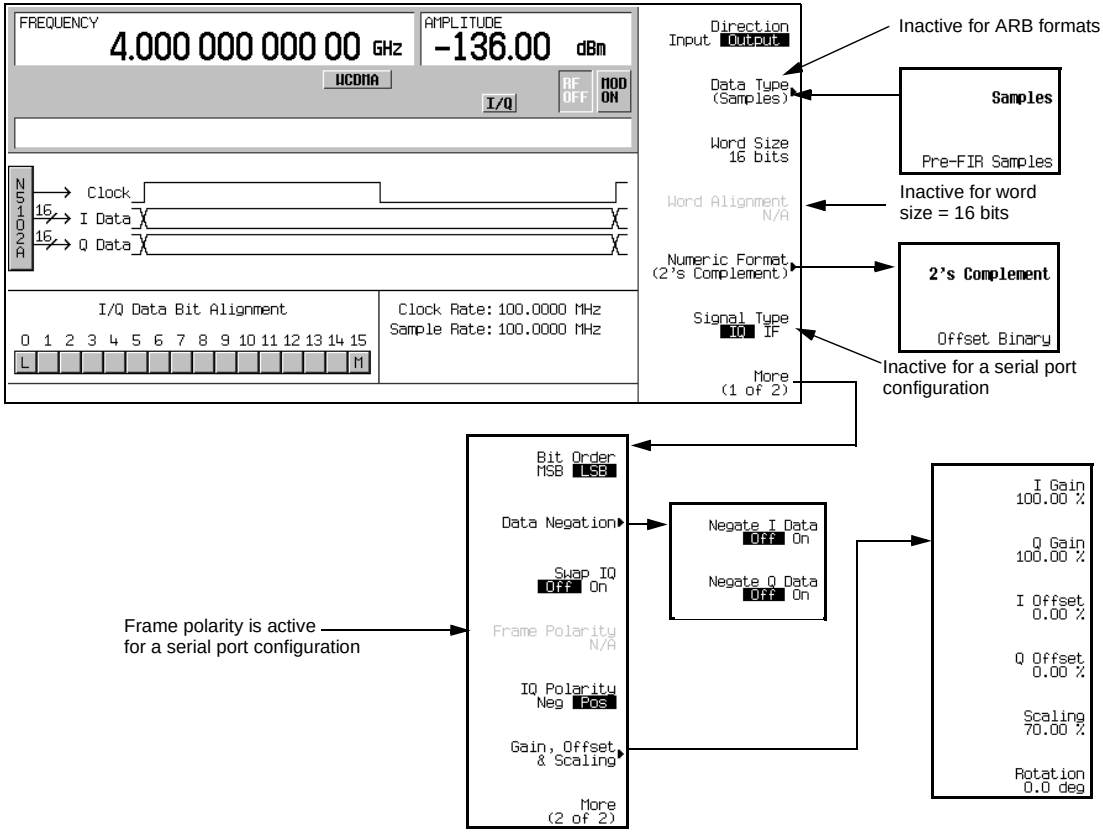
1. Refer to Figure 4-11. Press the **Data Setup** softkey.

Figure 4-11 Data Setup Menu Location



This softkey menu accesses the various parameters that govern the data received by the device under test. The status area of the display shows the number of data lines used for both I and Q along with the clock position relative to the data. When the port configuration is parallel or parallel interleaved, the number of data lines indicated is equivalent to the word (sample) size. When the port configuration is serial, the display will show that only one I and one Q data line is being used along with the frame marker that delineates the beginning of a sample. Figure 4-12 shows the data setup menu structure.

Figure 4-12 Data Setup Softkey Menu with Parallel Port Configuration



2. If a real-time modulation format is being used, press the **Data Type** softkey. (This softkey is inactive when an ARB modulation format is turned on.)

   In this menu, select whether the real-time baseband data from the signal generator is either filtered (**Samples**) or unfiltered (**Pre-FIR Samples**). The selection is dependent on the test needs. The **Samples** selection provides FIR filtered baseband samples according to the communication standard of the active modulation format. This is the preset selection and the one most commonly used. However if the device being tested already incorporates FIR filters, the **Pre-FIR Samples** selection should be used to avoid double filtering.

3. Select the data type that is appropriate for the test.

4. Press the **Numeric Format** softkey.

   From this menu, select how the binary values are represented. Selecting 2's complement allows both positive and negative data values. Use the Offset Binary selection when components cannot process negative values.

5. Select the numeric format required for the test.
6. Press the **More (1 of 2)** softkey.

   From this softkey menu, select the bit order, swap I and Q, select the polarity of the transmitted data, and access menus that provide data negation, scaling, gain, offset, and IQ rotation adjustments.
7. Press the **Data Negation** softkey.

   Negation differs from changing the I and Q polarity. Applied to a sample, negation changes the affected sample by expressing it in the two's complement form, multiplying it by negative one, and converting the sample back to the selected numeric format. This can be done for I samples, Q samples, or both.

   The choice to use negation is dependent on the device being tested and how it needs to receive the data.
8. Press the **Gain, Offset & Scaling** softkey.

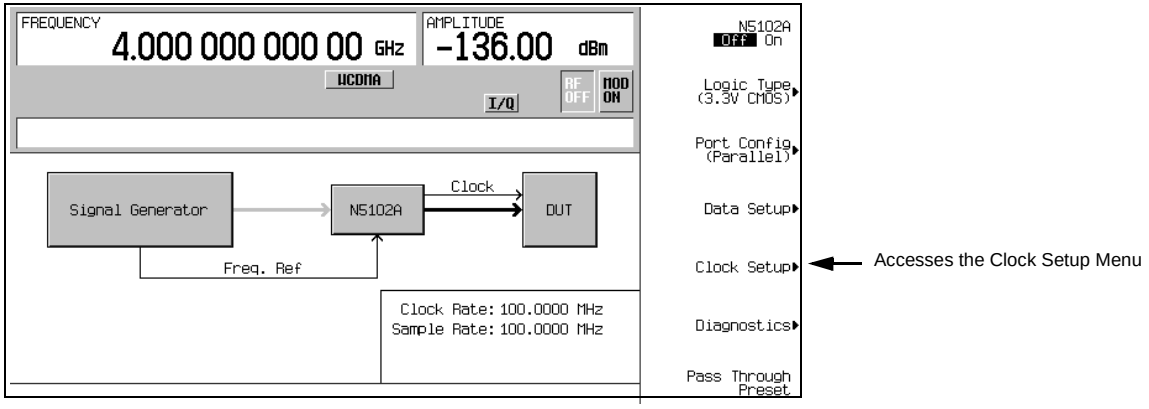
   Use the softkeys in this menu for the following functions:

   - reduce sample values for both I and Q using the **Scaling** softkey
   - increase or decrease the sample values independently for I and Q using the **I Gain** and **Q Gain** softkeys
   - compensate for or add a DC offset using the **I Offset** and **Q Offset** softkeys
   - rotate the data on the IQ plane using the **Rotation** softkey
9. Make any required scaling, gain, offset, or rotation adjustments to properly test the device.
10. Press **Return** > **Return** to return to the first-level softkey menu.

Configuring the Clock Signal

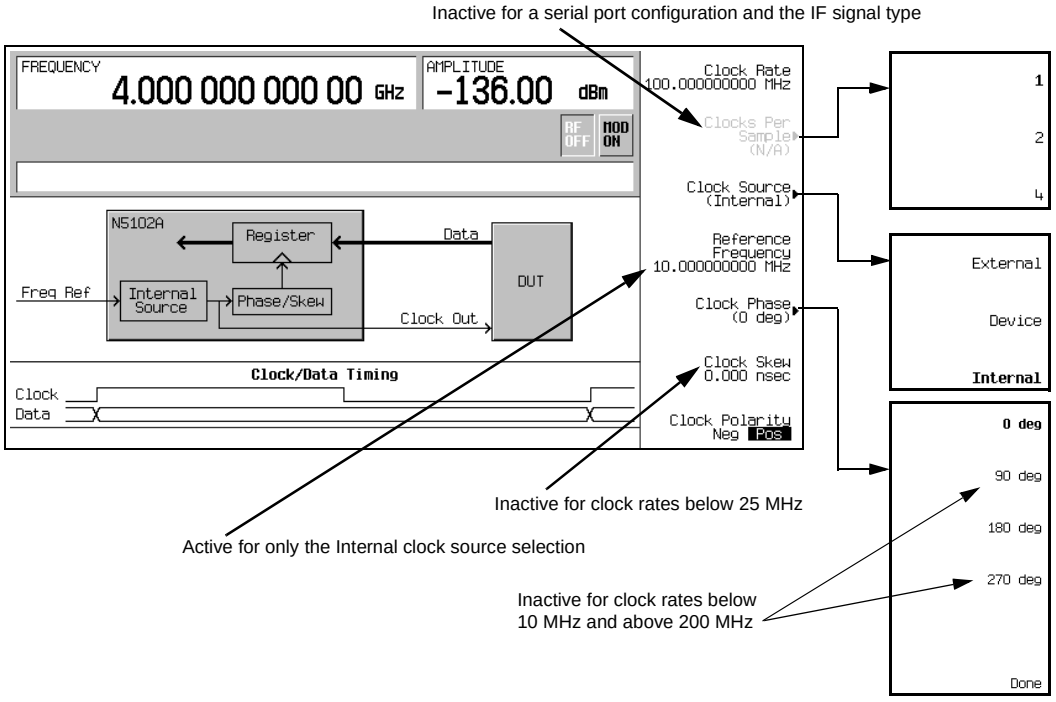
1. Refer to Figure 4-13. Press the **Clock Setup** softkey.

Figure 4-13 Clock Setup Menu Location



From this softkey menu, set all of the clock parameters that synchronize the clocks between the N5102A module and the ESG/PSG. You can also change the clock signal phase so the clock occurs during the valid portion of the data. Figure 4-14 shows the clock setup menu.

Figure 4-14 Clock Setup Softkey Menu for a Parallel Port Configuration



The top graphic on the display shows the current clock source that provides the output clock signal at the Clock Out and Device Interface connectors. The graphic changes to reflect the clock source selection discussed later in this procedure. The bottom graphic shows the clock position relative to the data. The displayed clock signal will change to reflect the following:

- clocks per sample selection
- clock phase choice
- clock skew adjustment
- clock polarity selection

If the device or external clock does not match the frequency, one of the following error messages will appear on the ESG/PSG:

```
805     Digital module output FIFO overflow error; There are more samples being
        produced than can be consumed at the current clock rate. Verify that
        the digital module clock is set up properly.
```

This error is reported when the output FIFO is overflowing in the digital module. This error can be generated if an external clock or its reference is not set up properly, or if the internal VCO is unlocked.

806 Digital module output FIFO underflow error; There are not enough samples being produced for the current clock rate. Verify that the digital module clock is set up properly.

This error is reported when the output FIFO is underflowing in the digital module. This error can be generated if an external clock or its reference is not set up properly, or if the internal VCO is unlocked.

2. If the port configuration is parallel or parallel interleaved, using an IQ signal type, press the **Clocks Per Sample** softkey.

   Notice that multiple clocks per sample can be selected. Some DACs require the ability to clock multiple times for each sample; having a clocks per sample value greater than one reduces the sample rate by a factor equal to the selected number of clocks per sample. The sample rate is viewed on the first-level and Data Setup softkey menus.

3. Select the clocks per sample value to fit the test.
4. Press the **Clock Source** softkey.

   From this menu, select the clock signal source. With each selection, the clock routing display in the signal generator clock setup menu will change to reflect the current clock source. This will be indicated by a change in the graphic.

5. Select the clock source.

   If External or Device is Selected

   Press the **Clock Rate** softkey and enter the clock rate of the externally applied clock signal.

NOTE The clock phase and clock skew may need to be adjusted any time the clock rate setting is changed. Refer to "Clock Timing for Phase and Skew Adjustments" on page 56.

For the **External** selection, the signal is supplied by an external clock source and applied to the Ext Clock In connector. For the **Device** selection, the clock signal is supplied through the Device Interface connector, generally by the device under test.

If Internal is Selected

Using an external frequency reference, the N5102A module generates its own internal clock signal. The reference frequency signal must be applied to the Freq Ref connector on the digital module.

a. Press the **Reference Frequency** softkey and enter the frequency of the externally applied frequency reference.

b. Press the **Clock Rate** softkey and enter the appropriate clock rate.

Table 4-8 provides a quick view of the settings and connections associated with each clock source selection.

Table 4-8 Clock Source Settings and Connectors

Clock Source	Softkeys		N5102A Module Connection		
	Reference Frequency	Clock Rate[1]	Freq Ref	Ext Clock In	Device Interface
External		●		●	
Device		●			●
Internal[2]	●	●	●		

1. For the Internal selection, this sets the internal clock rate. For the External and Device selections, this tells the interface module the rate of the applied clock signal.
2. There should be no clock signal applied to the Ext Clock In connector.

6. Press the **Clock Phase** softkey.

   From the menu that appears, you can adjust the phase of the clock relative to the data in 90 degree increments. The selections provide a coarse adjustment for positioning the clock on the valid portion of the data. Selecting 180 degrees is the same as selecting a negative clock polarity.

   The 90 degree and 270 degree selections are not available when the clock rate is set below 10 MHz or above 200 MHz. If 90 degrees or 270 degrees is selected when the clock rate is set below 10 MHz or above 200 MHz, the phase will change to 0 degrees or 180 degrees, respectively.

NOTE The clock phase and clock skew may need to be adjusted any time the clock rate setting is changed. Refer to "Clock Timing for Phase and Skew Adjustments" on page 56.

7. Enter the required phase adjustment.
8. Press the **Return** softkey to return to the clock setup menu.
9. Press the **Clock Skew** softkey.

   This provides a fine adjustment for the clock relative to its current phase position. The skew is a phase adjustment using increments of time. This enables greater skew adjustment capability at higher clock rates. For clock rates below 25 MHz, this softkey is inactive.

   The skew has discrete values with a range that is dependent on the clock rate. Refer to "Clock Timing for

Phase and Skew Adjustments" on page 56 for more information on skew settings.

10. Enter the skew adjustment that best positions the clock with the valid portion of the data.
11. Press the **Clock Polarity Neg Pos** softkey to Neg.

    This shifts the clock signal 180 degrees, so that the data starts during the negative clock transition. This has the same affect as selecting the 180 degree phase adjustment.
12. Make the clock polarity selection that is required for the device being tested.
13. Press the **Return** hardkey to return to the first-level softkey menu.

    The clock source selection is also reflected in the first-level softkey menu graphic. For example, if the device is the new clock source, the graphic will show that the frequency reference is now connected to the DUT and the DUT has an input clock line going to the N5102A module.

Generating Digital Data

Press the **N5102A Off On** softkey to On.

Digital data is now being transferred through the N5102A module to the device. The green status light should be blinking. This indicates that the data lines are active. If the status light is solidly illuminated (not blinking), all the data lines are inactive. The status light comes on and stays on (blinking or solid) after the first time the N5102A module is turned on (**N5102A Off On** to On). The status light will stay on until the module is disconnected from its power supply.

The interface module can only be turned on while a modulation format is active. If the modulation format is turned off while the module is on, the module will turn off and an error will be reported.

NOTE If changes are made to the baseband data parameters, it is recommended that you first disable the digital output (**N5102A Off On** softkey to Off) to avoid exposing your device and the N5102A module to the signal variations that may occur during the parameter changes.

Operating the N5102A Module in Input Mode

This section shows how to set the parameters for the N5102A module using the signal generator UI in the input direction. Each procedure contains a figure that shows the softkey menu structure for the interface module function being performed.

Refer to "Connecting the Clock Source and the Device Under Test" on page 60 and configure the test setup.

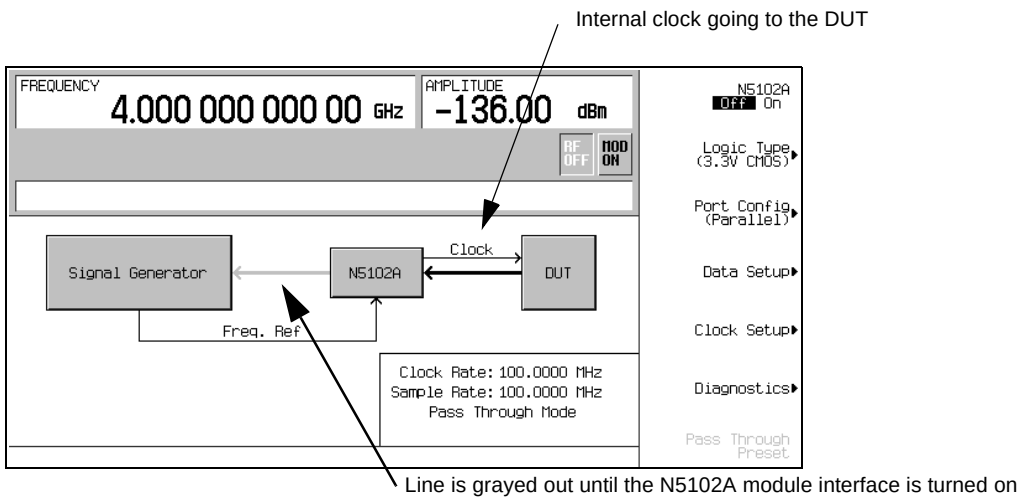
Accessing the N5102A Module User Interface

All parameters for the N5102A module are set with softkeys on the ESG/PSG signal generator.

Press **Aux Fctn** > **N5102A Interface**.

This accesses the UI (first-level softkey menu shown in Figure 4-15) that is used to configure the digital signal interface module. Notice the graphic, in the ESG/PSG display, showing a setup where the N5102A module is generating its own internal clock signal. This graphic changes to reflect the current clock source selection.

Figure 4-15 First-Level Softkey Menu



Selecting the Input Direction

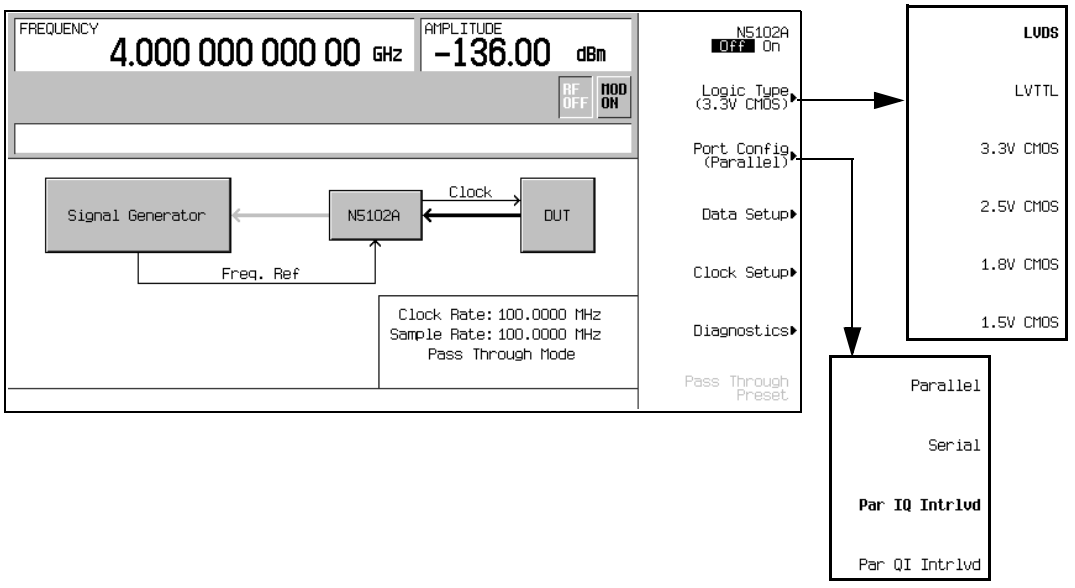
If both Option 003 (output mode) and Option 004 (input mode) are installed, you must select the input direction.

Press **Data Setup** > **Direction Input Output** to Input and press **Return**.

NOTE If only Option 004 is installed, the direction softkey will be unavailable and the mode will always be input.

Choosing the Logic Type and Port Configuration

Figure 4-16 Logic and Port Configuration Softkey Menus



1. Refer to Figure 4-16. Press the **Logic Type** softkey.

   From this menu, choose a logic type.

CAUTION Changing the logic type can increase or decrease the signal voltage level. To avoid damaging the device and/or the N5102A module, ensure that both are capable of handling the voltage change.

2. Select the logic type required for the device being tested.

   A caution message is displayed whenever a change is made to the logic types, and a softkey selection appears asking for confirmation.

3. Refer to Figure 4-16. Press the **Port Configuration** softkey.

   In this menu, select either a serial, parallel, or parallel interleaved data transmission.

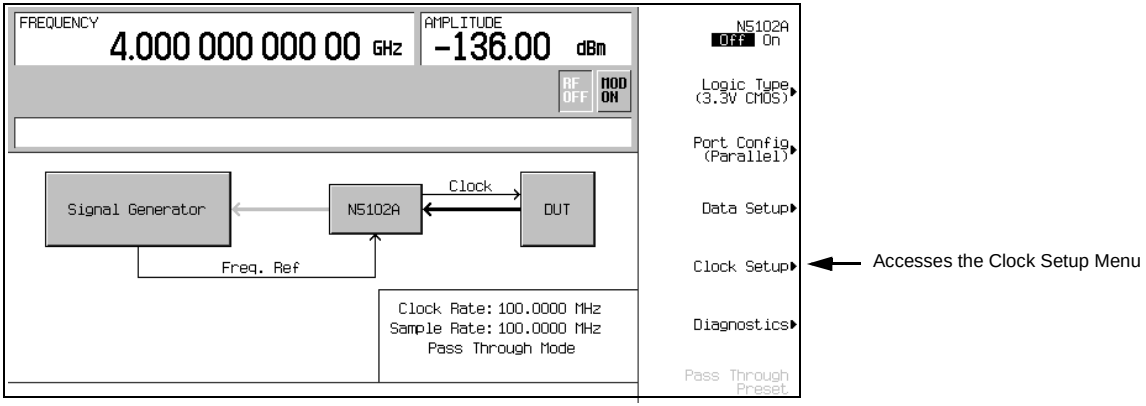
NOTE Within the data and clock setup softkey menus, some softkeys function relative to the current configuration. Softkeys that are grayed out are not available for the current setup. Refer to the help text to determine which parameter is causing the softkey to be unavailable. Press the **Help** hardkey on the ESG/PSG front panel and then the softkey that is unavailable.

4. Select the port configuration for the device being tested.

Configuring the Clock Signal

1. Refer to Figure 4-17. Press the **Clock Setup** softkey.

Figure 4-17 Clock Setup Menu Location



From this softkey menu, set all of the clock parameters that synchronize the data between the N5102A module and the device. From this menu, the clock signal phase can be changed so the clock occurs during the valid portion of the data. Figure 4-18 shows the clock setup menu.

If the device or external clock does not match the frequency, one of the following error messages will appear on the ESG/PSG:

803 `Digital module input FIFO overflow error; There are more samples being produced than can be consumed at the current clock rate. Verify that the digital module clock is set up properly.`

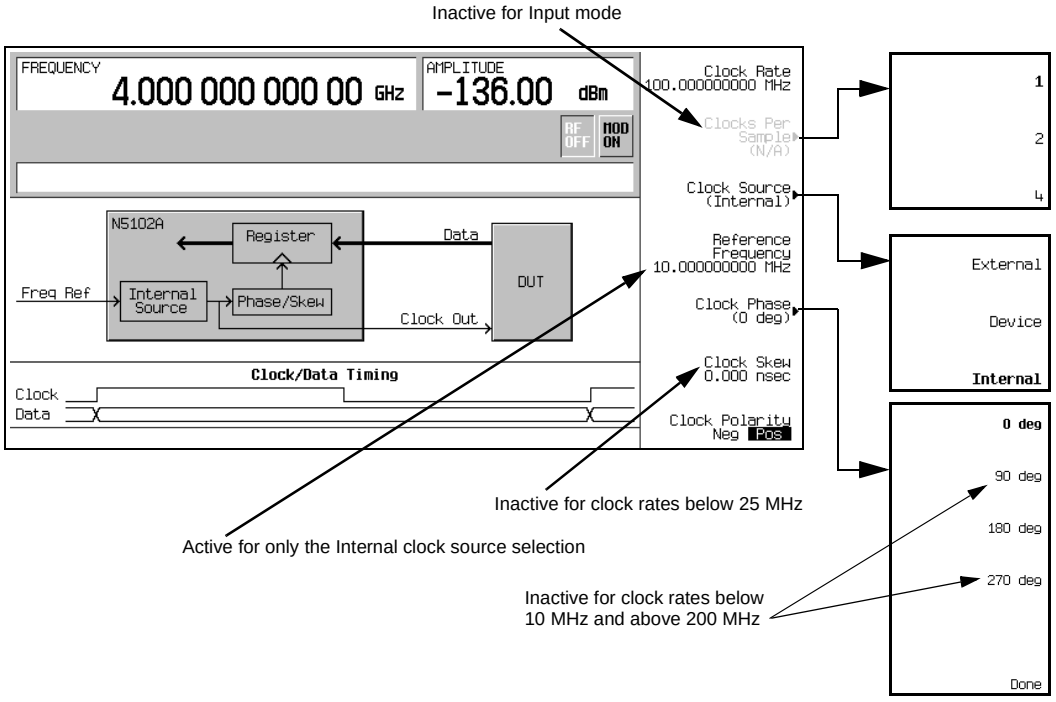
This error is reported when the digital module clock setup is not synchronized with the rate the samples are entering the digital module. Verify that the input clock rate matches the specified clock rate under the clock setup menu.

804 `Digital module input FIFO underflow error; There are not enough samples`

```
being produced for the current clock rate. Verify that the digital
module clock is set up properly.
```

This error is reported when the digital module clock setup is not synchronized with the rate the samples are entering the digital module. Verify that the input clock rate matches the specified clock rate under the clock setup menu.

Figure 4-18 Clock Setup Softkey Menu for a Parallel Port Configuration



The top graphic on the display shows the current clock source that provides the output clock signal at the Clock Out and Device Interface connectors. The graphic changes to reflect the clock source selection discussed later in this procedure. The bottom graphic shows the clock edges relative to the data. The displayed clock signal will change to reflect the following:

- clock phase choice
- clock skew adjustment
- clock polarity selection

2. Press the **Clock Source** softkey.

From this menu, select the clock signal source. With each selection, the clock routing display in the signal generator clock setup menu will change to reflect the current clock source. This will be indicated by a change in the graphic.

3. Select the clock source.

If External or Device is Selected

Press the **Clock Rate** softkey and enter the clock rate of the externally applied clock signal.

NOTE The clock phase and clock skew may need to be adjusted any time the clock rate setting is changed. Refer to "Clock Timing for Phase and Skew Adjustments" on page 56.

For the **External** selection, the signal is supplied by an external clock source and applied to the Ext Clock In connector. For the **Device** selection, the clock signal is supplied through the Device Interface connector, generally by the device being tested.

If Internal is Selected

Using an external frequency reference, the N5102A module generates its own internal clock signal. The reference frequency signal must be applied to the Freq Ref connector on the digital module.

a. Press the **Reference Frequency** softkey and enter the frequency of the externally applied frequency reference.

b. Press the **Clock Rate** softkey and enter the appropriate clock rate.

Table 4-9 provides a quick view of the settings and connections associated with each clock source selection.

Table 4-9 Clock Source Settings and Connectors

Clock Source	Softkeys		N5102A Module Connection		
	Reference Frequency	Clock Rate[1]	Freq Ref	Ext Clock In	Device Interface
External		●		●	
Device		●			●
Internal[2]	●	●	●		

1. For the Internal selection, this sets the internal clock rate. For the External and Device selections, this tells the interface module the rate of the applied clock signal.
2. There should be no clock signal applied to the Ext Clock In connector when Internal is being used.

4. Press the **Clock Phase** softkey.

From the menu that appears, the phase of the clock relative to the data can be changed in 90 degree increments. The selections provide a coarse adjustment for positioning the clock on the valid portion of the data. Selecting 180 degrees is the same as selecting a negative clock polarity.

The 90 degree and 270 degree selections are not available when the clock rate is set below 10 MHz or above 200 MHz. If 90 degrees or 270 degrees is selected when the clock rate is set below 10 MHz or above 200 MHz, the phase will change to 0 degrees or 180 degrees, respectively.

NOTE The clock phase and clock skew may need to be adjusted any time the clock rate setting is changed. Refer to "Clock Timing for Phase and Skew Adjustments" on page 56.

5. Enter the required phase adjustment.
6. Press the **Return** softkey to return to the clock setup menu.
7. Press the **Clock Skew** softkey.

   This provides a fine adjustment for the clock relative to its current phase position. The skew is a phase adjustment using increments of time. This enables greater skew adjustment capability at higher clock rates. For clock rates below 25 MHz, this softkey is inactive.

   The skew has discrete values with a range that is dependent on the clock rate. Refer to "Clock Timing for Phase and Skew Adjustments" on page 56 for more information on skew settings.
8. Enter the skew adjustment that best positions the clock with the valid portion of the data.
9. Press the **Clock Polarity Neg Pos** softkey to Neg.

   This shifts the clock signal 180 degrees, so that the data starts during the negative clock transition. This has the same affect as selecting the 180 degree phase adjustment.
10. Make the clock polarity selection that is required for the device being tested.
11. Press the **Return** hardkey to return to the first-level softkey menu.

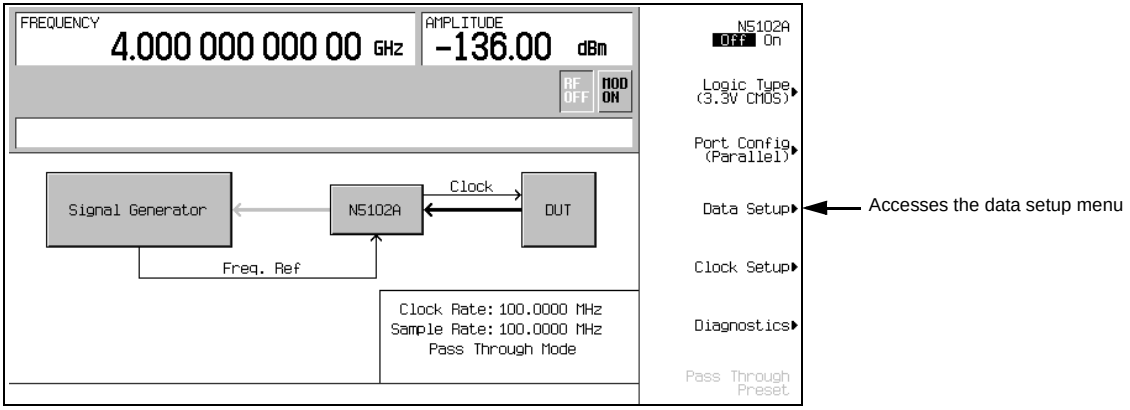
    The clock source selection is also reflected in the first-level softkey menu graphic. For example, if the device is the new clock source, you will see that the frequency reference is now connected to the DUT and the DUT has an input clock line going to the N5102A module.

Selecting the Data Parameters

This procedure guides you through the data setup menu. Softkeys that have self-explanatory names are generally not mentioned. For example, the **Word Size** softkey. For more information on all of the softkeys, refer to "Softkey and SCPI Command Descriptions" on page 84.

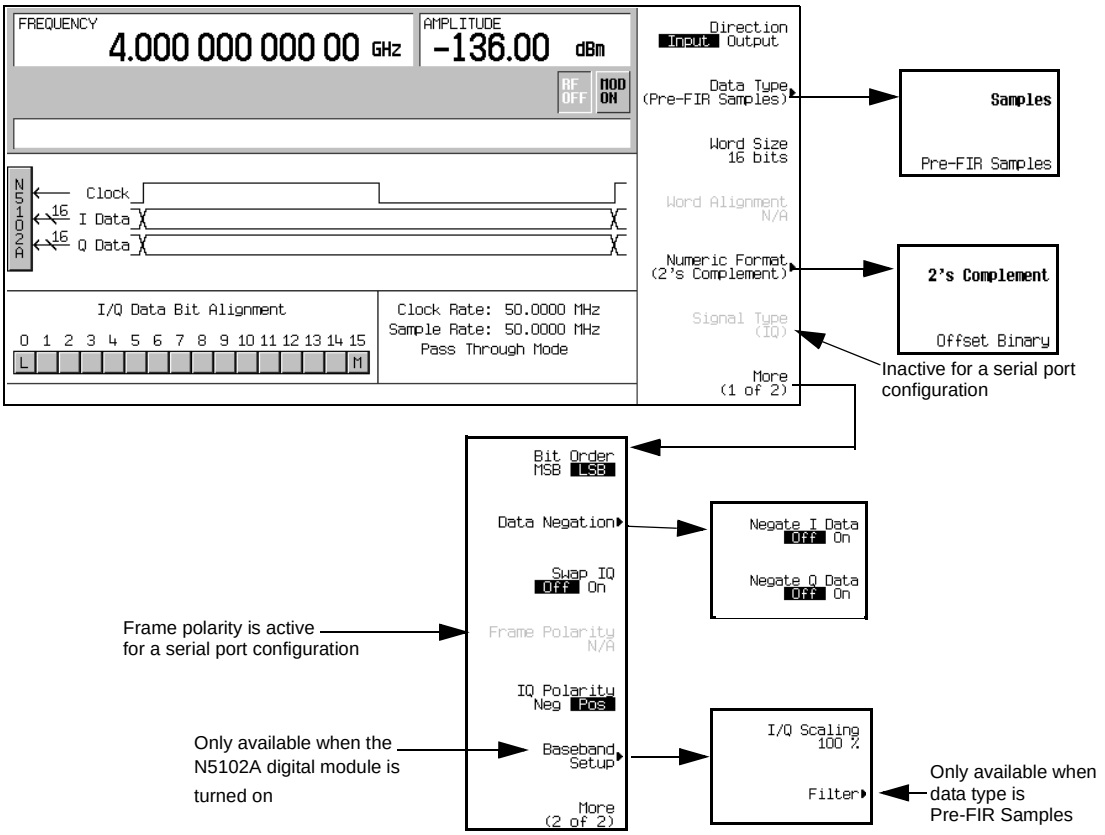
1. Refer to Figure 4-19. Press the **Data Setup** softkey.

Figure 4-19 Data Setup Menu Location



This softkey menu accesses the various parameters that govern the data received by the ESG/PSG The status area of the display shows the number of data lines used for both I and Q along with the clock position relative to the data. Figure 4-20 shows the data setup menu structure.

Figure 4-20 Data Setup Softkey Menu with Parallel Port Configuration



2. Press the **Data Type** softkey.

   In this menu, select the data type to be either filtered (**Samples**) or unfiltered (**Pre-FIR Samples**). The selection is dependent on the test needs and the device under test. However if the device being tested already incorporates FIR filters, the **Pre-FIR Samples** selection should be used to avoid double filtering. Refer to "Data Types" on page 58, for more information.

3. Select the data type that is appropriate for the test needs.

4. Press the **Numeric Format** softkey.

   From this menu, select how the binary values are represented. Selecting 2's complement allows both positive and negative data values. Use the Offset Binary selection when components cannot process negative values.

5. Select the numeric format required for the test.

6. Press the **More (1 of 2)** softkey.

From this softkey menu, select the bit order, swap I and Q, the polarity of the data, and access menus that provides data negation, scaling, and filtering parameters.

7. Press the **Data Negation** softkey.

   Negation differs from changing the I and Q polarity. Applied to a sample, negation changes the affected sample by expressing it in the two's complement form, multiplying it by negative one, and converting the sample back to the selected numeric format. This can be done for I samples, Q samples, or both.

   The choice to use negation is dependent on the device being tested.

8. To access I/Q scaling and filter parameters, press **Return** > **N5102A Off On** to On. This will invoke the real time Custom format in the ESG/PSG baseband generator. This is needed to set the filter parameters when Pre-FIR Samples is selected as the data type.

9. Press the **Baseband Setup** softkey.

   Use this softkey menu to adjust the I/Q scaling and access filter parameters. If the selected data type is Samples, the **Filter** softkey is grayed out (inactive). For more information on filtering, refer to the *Agilent ESG Vector Signal Generator User's Guide*, and for the PSG, refer to the *Agilent PSG Signal Generators User's Guide*.

Digital Data

If the N5102A digital module is not on, press **Return** > **Return** > **N5102A Off On** to On.

Digital data is now being transferred through the N5102A module to the ESG/PSG. The green status light should be blinking. This indicates that the data lines are active. If the status light is solidly illuminated (not blinking), all the data lines are inactive. The status light comes on and stays on (blinking or solid) after the first time the N5102A module is turned on (**N5102A Off On** to On). The status light will stay on until the module is disconnected from its power supply.

NOTE If changes are made to the baseband data parameters, it is recommended that you first disable the digital output (**N5102A Off On** softkey to Off) to avoid exposing the device and the N5102A module to the signal variations that may occur during the parameter changes.

Error Messages

If the N5102A digital signal interface module generates an error, the error will be reported on the ESG/PSG front panel. Errors are reported to both the front panel display error queue and the SCPI (remote interface) error queue. When an error occurs, a star (*) appears on the ESG/PSG display. If the error is intermittent, the star will disappear after on second. When the error is a persistent one, the star will remain on the display until the error is cleared.

The following is a list of some of the errors that may be generated by the digital module. A complete list is on the N5102A Baseband Studio digital module CD.

801 `Digital module VCO unlock error; The VCO on the digital module is unlocked. Check to make sure the clock settings are correct and the correct clock reference is connected.`

The VCO on the digital module is unlocked. Check to make sure the clock settings are correct and the correct clock reference is connected.

802 `Digital module overrange error; The output data is being clipped by the resampler. Reduce the scaling under the data menu to correct this problem.`

This error is reported when the output of the resampler is being clipped.

803 `Digital module input FIFO overflow error; There are more samples being produced than can be consumed at the current clock rate. Verify that the digital module clock is set up properly.`

This error is reported when the digital module clock setup is not synchronized with the rate the samples are entering the digital module. Verify that the input clock rate matches the specified clock rate under the clock setup menu.

804 `Digital module input FIFO underflow error; There are not enough samples being produced for the current clock rate. Verify that the digital module clock is set up properly.`

This error is reported when the digital module clock setup is not synchronized with the rate the samples are entering the digital module. Verify that the input clock rate matches the specified clock rate under the clock setup menu.

805 `Digital module output FIFO overflow error; There are more samples being produced than can be consumed at the current clock rate. Verify that the digital module clock is set up properly.`

This error is reported when the output FIFO is overflowing in the digital module. This error can be generated if an external clock or its reference is not set up properly, or if the internal VCO is unlocked.

806 `Digital module output FIFO underflow error; There are not enough samples being produced for the current clock rate. Verify that the digital module clock is set up properly.`

This error is reported when the output FIFO is underflowing in the digital module. This error can be generated if an external clock or its reference is not set up properly, or if the internal VCO is unlocked.

808 `Digital module unlock error; The output clock is not locked. The clock output may not be valid. Please make sure all references and clocks are connected and the module is set up properly.`

This occurs when the output clock modules are not locked. This can occur when the externally supplied clock is not stable, the module is not set up properly, or the internal clock is not locked. If the error persists after fixing all external causes, then the module may need to be reset by turning it off then on. This will set up the clock modules properly.

809 `Digital module missing clock; Please make sure the external clock is connected and the clock settings are correct.`

This error occurs when the output clock modules are not receiving a clock. This usually happens when the external or Device clock source is selected and there is no clock source connected to the clock input. If the error persists after fixing all external causes, then the module may need to be reset by turning it off then on. This will set up the clock modules properly.

5 Softkeys and SCPI Commands

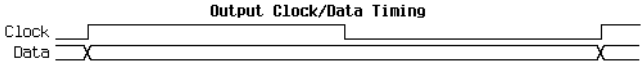
This chapter describes the softkeys and SCPI commands for the N5102A Baseband Studio digital signal interface module. Softkeys and SCPI commands that perform the same function are documented together.

Softkey and SCPI Command Descriptions

0 deg

This softkey aligns the transition edge of the clock with the beginning of each sample for parallel or parallel interleaved data transmission and with each bit for a serial data transmission. This is the factory preset phase selection.

Figure 5-1 Clock Relative to the Data at 0 Degrees



SCPI
```
:DIGital:CLOCk:PHASe 0
:DIGital:CLOCk:PHASe?
```

1

For a parallel or parallel interleaved port configuration, this softkey selects one clock per sample. This is the factory preset selection. With either a serial port configuration or an IF signal type, or when in input mode, this softkey is not accessible.

SCPI
```
DIGital:CLOCk:CPS 1
Digital:CLOCk:CPS?
```

If this command is executed with a serial port configuration or an IF signal type, the parameter value is changed, but it is not used by the interface module until the port configuration is changed to parallel or parallel interleaved, *and* the signal type is changed to IQ.

Because a query returns the currently set value, regardless of the port configuration, you must query all four states (clocks per sample, port configuration, data direction, and signal type) to know the interface module's current setup.

1.5V CMOS

This softkey sets the N5102A module logic type to a 1.5 volt CMOS signal.

CAUTION Changing the logic type changes the voltage levels. To avoid potential damage to your device or the N5102A module, first verify that the new logic type and voltage are appropriate.

SCPI
```
:DIGital:LOGic[:TYPE] CMOS15
:DIGital:LOGic[:TYPE]?
```

1.8V CMOS

This softkey sets the N5102A module logic type to a 1.8 volt CMOS signal.

CAUTION Changing the logic type changes the voltage levels. To avoid potential damage to your device or the N5102A module, first verify that the new logic type and voltage are appropriate.

SCPI
```
:DIGital:LOGic[:TYPE] CMOS18
:DIGital:LOGic[:TYPE]?
```

2

For a parallel or parallel interleaved port configuration in the output mode, this softkey selects two clocks per sample. With either a serial port configuration, or an IF signal type, this softkey is not accessible.

SCPI
```
DIGital:CLOCk:CPS 2
DIGital:CLOCk:CPS?
```

If this command is executed with a serial port configuration or an IF signal type, the parameter value is changed, but it is not used by the interface module until the port configuration is changed to parallel or parallel interleaved, *and* the signal type is changed to IQ.

Because a query returns the currently set value, regardless of the port configuration, you must query all four states (clocks per sample, port configuration, data direction, and signal type) to know the interface module's current setup.

2's Complement

This softkey sets the N5102A module data format to a two's complement representation of the data values. This is the factory preset selection.

SCPI
```
:DIGital:DATA:NFORmat TCOMplement
:DIGital:DATA:NFORmat?
```

2.5V CMOS

This softkey sets the N5102A module logic type to a 2.5 volt CMOS signal.

CAUTION Changing the logic type changes the voltage levels. To avoid potential damage to your device or the N5102A module, first verify that the new logic type and voltage are appropriate.

SCPI
```
:DIGital:LOGic[:TYPE] CMOS25
:DIGital:LOGic[:TYPE]?
```

3.3V CMOS

This softkey sets the N5102A module logic type to a 3.3 volt CMOS signal. This is the factory preset logic type.

CAUTION Changing the logic type changes the voltage levels. To avoid potential damage to your device or the N5102A module, first verify that the new logic type and voltage are appropriate.

SCPI
```
:DIGital:LOGic[:TYPE] CMOS33
:DIGital:LOGic[:TYPE]?
```

4

For a parallel or parallel interleaved port configuration in the output mode, this softkey selects four clocks per sample. With either a serial port configuration, or an IF signal type, this softkey is not accessible.

SCPI
```
DIGital:CLOCk:CPS 4
DIGital:CLOCk:CPS?
```

If this command is executed with a serial port configuration or an IF signal type, the parameter value is changed, but it is not used by the interface module until the port configuration is changed to parallel or parallel interleaved, *and* the signal type is changed to IQ.

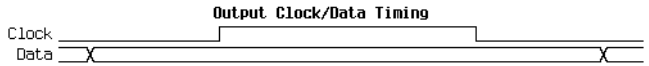
Because a query returns the currently set value, regardless of the port configuration, you must query all four states (clocks per sample, port configuration, data direction, and signal type) to know the interface module's current setup.

90 deg

This softkey provides a 90 degree phase adjustment for the clock signal. The phase adjustment moves the clock transition edge relative to the beginning of each sample for parallel or parallel interleaved data transmission and to each bit during a serial data transmission.

This softkey is grayed out (unavailable) when the clock rate is less than 10 MHz or greater than 200 MHz. If 90 degrees is the phase setting when the clock rate is changed to a value that is less than 10 MHz or greater than 200 MHz, the phase setting becomes zero degrees.

Figure 5-2 Clock Relative to the Data at 90 Degrees



SCPI
```
:DIGital:CLOCk:PHASe 90
:DIGital:CLOCk:PHASe?
```

If this command is executed when the clock rate is less than 10 MHz or greater than 200 MHz, the resolution of this setting changes to 180 degrees, and the maximum phase becomes 180 degrees.

180 deg

This softkey provides a 180 degree phase adjustment for the clock signal. The phase adjustment is relative to the beginning of each sample for a parallel or parallel interleaved data transmission and to each bit during a serial data transmission. This functions the same as selecting the negative clock polarity using the **Clock Polarity Neg Pos** softkey.

Figure 5-3 Clock Relative to the Data at 180 Degrees

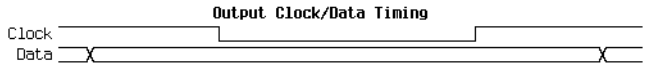
SCPI
```
:DIGital:CLOCk:PHASe 180
:DIGital:CLOCk:PHASe?
```

270 deg

This softkey provides a 270 degree phase adjustment for the clock signal. The phase adjustment moves the clock transition edge relative to the beginning of each sample for parallel or parallel interleaved data transmission and to each bit during a serial data transmission.

This softkey is grayed out (unavailable) when the clock rate is less than 10 MHz or greater than 200 MHz. If 270 degrees is the phase setting when the clock rate is changed to a value that is less than 10 MHz or greater than 200 MHz, the phase becomes 180 degrees.

Figure 5-4 Clock Relative to the Data at 270 Degrees



SCPI
```
:DIGital:CLOCk:PHASe 270
:DIGital:CLOCk:PHASe?
```

If this command is executed when the clock rate is less than 10 MHz or greater than 200 MHz, the resolution of this setting changes to 180 degrees, and the maximum phase becomes 180 degrees.

Baseband Setup

This softkey accesses a menu that enables you to adjust the scaling of the IQ data, and select filtering when the data type is Pre-FIR Samples. This menu is only available in the Input mode. For more information on scaling and filtering, refer to "Custom Real Time I/Q Baseband" in the *Agilent ESG Vector Signal Generator User's Guide* or the *Agilent PSG Signal Generators User's Guide*.

Bit Order MSB LSB

This softkey selects the bit ordering of the data that is transmitted through the N5102A module.

MSB — This selection transmits the most significant bit (MSB) on data line zero for both I and Q for a parallel or parallel interleaved port configuration, and transmits the MSB as the first bit in a sample for a serial port configuration.

LSB — This selection transmits the least significant bit (LSB) on data line zero for both I and Q for a parallel or parallel interleaved port configuration, and transmits the LSB as the first bit in a sample for a serial port configuration.

For information on selecting the port configuration, see "Port Config" on page 99.

Preset LSB

SCPI
```
:DIGital:DATA:BORDer MSB|LSB
:DIGital:DATA:BORDer?
```

Clock Phase

This softkey accesses a menu that enables you to select the phase adjustment (in 90 degree increments) of the clock edge relative to the start of each sample for a parallel or parallel interleaved data

transmission, and to each data bit for a serial data transmission.

In addition to making coarse adjustments, a fine-skew adjustment is available. See "Clock Skew" on page 89 for more information.

Preset 0 deg

SCPI
```
:DIGital:CLOCk:PHASe 0|90|180|270
:DIGital:CLOCk:PHASe?
```

When the clock rate is less than 10 MHz or greater than 200 MHz, the resolution of this setting changes from 90 degrees to 180 degrees, and the maximum phase becomes 180 degrees.

Clock Polarity Neg Pos

This softkey selects which clock edge (rising or falling) is aligned with the start of a sample for a parallel or parallel interleaved data transmission, and with the start of each bit for a serial data transmission. The Neg selection functions the same as selecting the 180 degree phase adjustment using the 180 deg softkey.

Preset Pos

SCPI
```
:DIGital:CLOCk:POLarity POSitive|NEGative
:DIGital:CLOCk:POLarity?
```

Clock Rate

This softkey enables you to adjust the clock rate (frequency) when the internal clock is used, or to enter the clock rate of an external clock source (connected at the Ext Clock In connector or supplied through the Device Interface connector). The value set with this softkey is also the rate for the output clock signal at the Clock Out connector and the Device Interface connector. See "Clock Source" on page 90 for information on selecting the clock source.

The clock rate range is dependent on the port configuration, logic type, signal type, and clocks per sample. Signal type and clocks per sample apply to parallel and parallel interleaved transmissions.

Preset 100.000000000 MHz

SCPI
```
:DIGital:CLOCk:RATE <val><unit>
:DIGital:CLOCk:RATE?
```

Clock Setup

This softkey accesses a menu that enables you to select the clock and external frequency reference parameters that are used to synchronize the transmitted data.

Clock Skew

This softkey provides a fine-adjustment for aligning the clock to the valid portion of the data relative

to the coarse adjustment associated with the **Clock Phase** softkey. Because this is a fine adjustment, it provides greater benefit at higher clock rates. When the clock rate is less than 25 MHz, this softkey is grayed out (inactive).Skew is displayed in nanoseconds with a maximum range and a maximum number of discrete steps. Both the range and the number of steps are variable, and depend on the clock rate. The skew range decreases as the clock rate increases, and increases as the clock rate decreases. The maximum skew range is reached at a clock rate of approximately 99 MHz and is maintained down to a clock rate of 25 MHz.

Preset 0.000 ns

Range up to ±127 discrete steps, with a boundary of ±5 ns

$$\textit{Discrete Step Resolution: } \frac{1}{256 \times \text{Clock Rate}}$$

SCPI
```
:DIGital:CLOCk:SKEW <val><unit>
:DIGital:CLOCk:SKEW?
```

Clock Source

This softkey accesses a menu where the clock source is selected. The selected clock source also provides the output clock signal at the Clock Out and Device Interface connectors.

CAUTION It is important that the signal generator, the interface module, and the DUT are locked to a common frequency reference. Failure to have a common frequency reference may result in a loss of data. See "Common Frequency Reference" on page 48 for information.

Preset Internal

SCPI
```
:DIGital:CLOCk:SOURce EXTernal|DEVice|INTernal
:DIGital:CLOCk:SOURce?
```

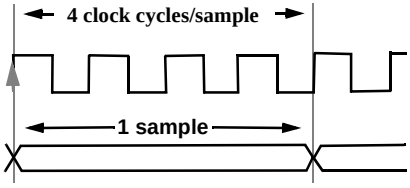
Clocks Per Sample

For a digital IQ signal, this softkey accesses a menu that enables you to select the number of clock cycles per sample, and is active for a parallel or parallel interleaved port configuration (see "Port Config" on page 99). For a serial port configuration or an IF signal, or while in input mode, this softkey is grayed out (inactive).

Some devices require multiple clocks per sample. The N5102A module provides multiple clocks per sample choices (1x, 2x, or 4x). When you select a clocks per sample that is greater than one, the sample is held for the selected number of clock cycles. This reduces the sample rate relative to the

clock rate by a factor equal to the clocks per sample value.

Example



For more information on clock rates, see "Clock Rate" on page 89.

Preset 1

SCPI `DIGital:CLOCk:CPS 1|2|4`
`DIGital:CLOCk:CPS?`

If this command is executed with a serial port configuration, an IF signal type, or input mode, the parameter value is changed, but it is not *used* by the signal generator until the port configuration is changed to parallel or parallel interleaved, *and* the signal type is changed to IQ.

Because a query returns the currently set value, regardless of the port configuration, you must query all states (clocks per sample, port configuration, data direction, and signal type) to know the signal generator's current setup.

Data Negation

This softkey accesses a menu that enables you to select either I or Q data negation. Negation changes the affected sample by expressing it in two's complement form, multiplying by negative one, and converting back to the selected numeric format.

Data Setup

This softkey accesses a menu that enables you to set the parameters for transmitted data.

Data Type

This softkey accesses a menu that enables you to select either filtered or unfiltered baseband data to be transmitted through the digital module.

When an ARB modulation format is on, this softkey is grayed out (inactive) and the data type is samples.

Preset Samples

SCPI `:DIGital:DATA:TYPE Samples|PFSamples`
`:DIGital:DATA:TYPE?`

If this command is executed while an ARB modulation format is active, the parameter choice is changed, but it is not *used* by the interface module until a real-time modulation format is turned on.

Because a query returns the current choice, regardless of whether or not an ARB format is active, you must query both states (data type and the modulation format) to know the signal generator's current setup.

Device

This softkey selects the external clock signal that is provided through the Device Interface connector as the clock source for the N5102A module. You must also set the interface module clock rate to match that of the external clock signal (see "Clock Rate" on page 89). With this selection, the supplied clock is available as an output clock signal at the Clock Out and Device Interface connectors on the N5102A module.

CAUTION It is important that the signal generator, the interface module, and the DUT are locked to a common frequency reference. Failure to have a common frequency reference may result in a loss of data. See "Common Frequency Reference" on page 48 for information.

SCPI `:DIGital:CLOCk:SOURce DEVice`
`:DIGital:CLOCk:SOURce?`

Device Intfc

This softkey selects a comprehensive loop back test that validates the delivery of digital data from the digital bus connector on the ESG/PSG to the Device Interface output connector on the N5102A module. This test requires the LOOP BACK TEST SINGLE ENDED IO DUAL 40 PIN board be connected to the interface module with no connections to the two 40 pin connectors.

Use this test to verify that the system is functioning properly after installation, or whenever the need arises. Running any loop back test turns off all active formats and the module. If this test fails, there are three other diagnostic tests that can help isolate the problem to the N5102A module, the digital bus cable, or the ESG/PSG. For information on these tests, see "SigGen Dig Bus" on page 102, "Dig Bus Cable" on page 93, and "N5102A Dig Bus" on page 96. To run the test, see "Run Loop Back Test" on page 101.

SCPI `:DIGital:DIAGnostic:LOOPback? DEVice`

This command executes the diagnostic test, and returns the results of the test as pass or fail.

Diagnostics

This softkey accesses a menu where you can select and run N5102A module loop back tests.

Dig Bus Cable

This softkey selects a loop back test that verifies the output capability from the ESG/PSG Digital Bus connector to the end of the digital bus cable. To run the test, see "Run Loop Back Test" on page 101.

SCPI `:DIGital:DIAGnostic:LOOPback? DCABLe`

This command executes the diagnostic test and returns the results of the test as pass or fail.

Direction Input Output

This softkey selects the direction of the data through the digital module.

SCPI `:DIGital:DATA:DIRection OUTPut|INPut`
`:DIGital:DATA:DIRection?`

External

This softkey selects the external clock signal provided through the Ext Clock In connector as the clock source for the N5102A module. You must also set the interface module clock rate to match that of the external clock signal (see "Clock Rate" on page 89). With this selection, the external clock is available as an output clock signal at the Clock Out and Device Interface connectors on the N5102A module.

CAUTION It is important that the signal generator, the interface module, and the device are locked to a common frequency reference. Failure to have a common frequency reference may result in a loss of data. See "Common Frequency Reference" on page 48 for information.

SCPI `:DIGital:CLOCk:SOURce EXTernal`
`:DIGital:CLOCk:SOURce?`

Filter

In Input mode, this softkey accesses a menu that enables you to select filtering parameters. This softkey is grayed out (inactive) unless Pre-FIR Samples is the selected data type.

Frame Polarity Neg Pos

This softkey sets the polarity of the frame marker that delineates the beginning of each sample during a serial data transmission.

Neg	The frame line is low while data for the first sample is available.
Pos	The frame line is high while data for the first sample is available.

The frame marker is not affected by phase and skew adjustments.

For a parallel port configuration, this softkey is grayed out (inactive). For information on selecting serial data, see "Port Config" on page 99.

Preset	Pos
SCPI	`:DIGital:DATA:POLarity:FRAMe NEGative|POSitive` `:DIGital:DATA:POLarity:FRAMe?`

If this command is executed with a parallel or parallel interleaved port configuration, the parameter value is changed, but it is not used by the signal generator until the port configuration is changed to serial.

Because a query returns the currently set value, regardless of the port configuration, you must query both states (frame polarity and port configuration) to know the signal generator's current setup.

Gain, Offset & Scaling

In Output mode, this softkey accesses a menu that enables you to adjust the gain, DC offset, scaling, and IQ rotation for the transmitted data.

I Gain

In Output mode, this softkey enables you to adjust the gain for the N5102A module I data. This is a fine adjustment that is independent of the Q data and can be used to complement the setting obtained using the **Scaling** softkey.

Preset	100.0%
Range	87.50–112.5%
SCPI	`:DIGital:DATA:IGain <val>` `:DIGital:DATA:IGain?`

I Offset

In Output mode, this softkey enables you to adjust the DC offset for the N5102A module I data. The offset can be used to compensate for an existing impairment or to introduce an impairment to the I data.

Preset	0.00%
Range	-100 to 100% of full scale
SCPI	`:DIGital:DATA:IOFFset <val>` `:DIGital:DATA:IOFFset?`

Internal

This softkey selects the N5102A module internal clock as the clock source. This requires that the same external reference frequency be applied to both the Freq Ref connector and the ESG/PSG. You must also set the interface module reference frequency to match that of the applied signal (see "Reference Frequency" on page 100). This is the factory preset clock source selection. With this selection, the internal clock signal is available at the Clock Out and Device Interface connectors on the N5102A module.

CAUTION It is important that the signal generator, the interface module, and the device are locked to a common frequency reference. Failure to have a common frequency reference may result in a loss of data. See "Common Frequency Reference" on page 48 for information.

SCPI
```
:DIGital:CLOCk:SOURce INTernal
:DIGital:CLOCk:SOURce?
```

IQ Polarity Neg Pos

This softkey sets the polarity of the I and Q data lines for the N5102A module.

Neg — The data on both the I and Q data lines are inverted. A digital one is represented by a low logic level at the output.

Pos — The polarity of the output data matches the input data. A digital one is represented by a high logic level at the output.

Preset — Pos

SCPI
```
:DIGital:DATA:POLarity:IQ POSitive|NEGative
:DIGital:DATA:POLarity:IQ?
```

I/Q Scaling

When in the Input mode, this softkey enables you to adjust the scaling of both the I and the Q data transmitted through the N5102A module. For Output mode, see "Scaling" on page 101.

Logic Type

This softkey accesses a menu that enables you to select the logic type for the N5102A module data.

CAUTION Changing the logic type changes the voltage levels. To avoid potential damage to your device or the N5102A module, first verify that the new logic type and voltage are appropriate.

Preset 3.3V CMOS

SCPI
```
:DIGital:LOGic[:TYPE] LVDS|LVTTl|CMOS33|CMOS25|
CMOS18|CMOS15
:DIGital:LOGic[:TYPE]?
```

Loop Back Test Type

This softkey accesses a menu where you can select different loop back tests to verify the operation of the ESG/PSG digital output and the N5102A module.

To run the tests, see "Run Loop Back Test" on page 101.

Preset Device Intfc

SCPI
```
:DIGital:DIAGnostic:LOOPback? DIGBus|CABLe|N5102A|DEVice
```

This command executes the selected diagnostic test and returns the results of the test as pass or fail.

LVDS

This softkey sets the logic type for the N5102A module to low voltage differential signaling (LVDS).

CAUTION Changing the logic type changes the voltage levels. To avoid potential damage to your device or the N5102A module, first verify that the new logic type and voltage are appropriate.

SCPI
```
:DIGital:LOGic[:TYPE] LVDS
:DIGital:LOGic[:TYPE]?
```

LVTTL

This softkey sets the logic type for the N5102A module to a low voltage TTL signal.

CAUTION Changing the logic type changes the voltage levels. To avoid potential damage to your device or the N5102A module, first verify that the new logic type and voltage are appropriate.

SCPI
```
:DIGital:LOGic[:TYPE] LVTTl
:DIGital:LOGic[:TYPE]?
```

N5102A Dig Bus

This softkey selects a loop back test that verifies the connection and data transfer capability between the ESG/PSG and the N5102A module. The loop back for this test occurs at the input of the N5102A

module and ensures that the Digital Bus input connector is functioning properly. For selecting the comprehensive test that includes verifying the operation of the N5102A module Device Interface output connector, see "Device Intfc" on page 92. To run the test, see "Run Loop Back Test" on page 101.

SCPI `:DIGital:DIAGnostic:LOOPback? N5102A`

This command executes the diagnostic test and returns the results of the test as pass or fail.

N5102A Interface

This softkey accesses menus that enable you to control and set the N5102A module parameters.

N5102A Off On

This softkey enables or disables the N5102A module.

In the output mode, the interface module can only be turned on while a modulation format is active. If the modulation format is turned off while the module is on, the module will turn off and an error will be reported.

When the N5102A Interface is on, the ESG/PSG continuously polls the N5102A module to ensure it is connected. If the ESG/PSG determines that the N5102A module is not connected, it reports an error. This also occurs if power is not supplied to the N5102A module via the included power supply. If the module is disconnected while on, the interface turns off and reports an error.

NOTE If the softkey selection is On while setting the ESG/PSG parameters, the device under test can be subject to all output variations that are produced by intermediate setting changes.

Preset Off

SCPI `:DIGital[:STATe] 0|1|OFF|ON`
`:DIGital[:STATe]?`

Negate I Data Off On

This softkey enables or disables negation of the value of each sample of the I data. Negation changes the affected sample by expressing it in two's complement form, multiplying by negative one, and converting back to the selected numeric format. This can be done for I samples, Q samples, or both.

On The I data is negated.

Off No negation is performed.

Preset Off

SCPI `:DIGital:DATA:INEGate 0|1|OFF|ON`

```
:DIGital:DATA:INEGate?
```

Negate Q Data Off On

This softkey enables or disables negation of the value of each sample of the Q data. Negation changes the affected sample by expressing it in two's complement form, multiplying by negative one, and converting back to the desired numeric format. This can be done for I samples, Q samples, or both.

On	The Q data is negated.
Off	No negation is performed.
Preset	Off
SCPI	`:DIGital:DATA:QNEGate 0|1|OFF|ON` `:DIGital:DATA:QNEGate?`

Numeric Format

This softkey accesses a menu that enables you to select the binary format (representation) for the data values that are transmitted. There are two binary format choices, 2's complement and offset binary.

Preset	2's Complement
SCPI	`:DIGital:DATA:NFORmat TCOMplement|OBINary` `:DIGital:DATA:NFORmat?`

Offset Binary

This softkey sets the N5102A module data format to an offset binary representation of the data values.

SCPI	`:DIGital:DATA:NFORmat OBINary` `:DIGital:DATA:NFORmat?`

Pass Through Preset

This softkey enables you to transmit data through the digital module with no modifications. The resample ratio is set to 1 by adjusting the clock rate to match the baseband sample rate and all of the formatting functions are set so that the data is not modified. This softkey is grayed out (inactive) until a modulation format is activated.

In input mode, the baseband clock rate is set to match the clock rate settings of the N5102A digital module.

SCPI	`:DIGital:PRESet:PTHRough`

Par IQ Intrlvd

This softkey enables parallel interleaving of the data samples transmitted, where the I sample is transmitted on the rising edge and the Q sample is transmitted on the falling edge.

For more information on parallel interleaved data transmissions, see "Clock Timing for Parallel Interleaved Data" on page 54.

SCPI `:DIGital:PCONFig PINTIQ`
`:DIGital:PCONFig?`

Par QI Intrlvd

This softkey enables parallel interleaving of the data samples transmitted, where the Q sample is transmitted on the rising edge and the I sample is transmitted on the falling edge.

For more information on parallel interleaved data transmissions, see "Clock Timing for Parallel Interleaved Data" on page 54.

SCPI `:DIGital:PCONFig PINTQI`
`:DIGital:PCONFig?`

Parallel

This softkey enables parallel data transmission. This is the factory preset port configuration.

SCPI `:DIGital:PCONFig PARallel`
`:DIGital:PCONFig?`

Pre-FIR Samples

This softkey selects unfiltered data as the data type to be transferred through the N5102A module. When an ARB modulation format is on, this softkey is not accessible. In the Input mode, this data type limits the clock rate to 50 MHz for filters with a width 16 symbols, and 25 MHz for filters with a symbol width.

SCPI `:DIGital:DATA:TYPE PFSamples`
`:DIGital:DATA:TYPE?`

If this command is executed while an ARB modulation format is active, the parameter choice is changed, but it is not *used* by the signal generator until a real-time modulation format is turned on.

Because a query returns the current choice, regardless of whether or not an ARB format is active, you must query both states (data type and the modulation format) to know the signal generator's current setup.

Port Config

This softkey accesses a menu that enables you to select a parallel, serial, parallel interleaved IQ, or parallel interleaved QI data transmission between the N5102A module and the DUT.

Preset Parallel

SCPI `:DIGital:PCONFig PARallel|SERial|PINTIQ|PINTQI`

```
:DIGital:PCONFig?
```

Q Gain

When in Output mode, this softkey enables you to adjust the gain for the N5102A module Q data. This is a fine adjustment, independent of the I data, that can be used to complement the setting obtained using the **Scaling** softkey.

Preset 100.0%

Range 87.50–112.5%

SCPI
```
:DIGital:DATA:QGain <val>
:DIGital:DATA:QGain?
```

Q Offset

When in Output mode, this softkey enables you to adjust the DC offset for the N5102A module Q data. The offset can be used to compensate for an existing impairment or to introduce an impairment to the Q data.

Preset 0.00%

Range –100 to 100% of full scale

SCPI
```
:DIGital:DATA:QOFFset <val>
:DIGital:DATA:QOFFset?
```

Reference Frequency

For the Internal source selection, this softkey enables you to specify the frequency of the external reference supplied to the Freq Ref connector. The specified frequency enables the internal source of the N5102A module to lock onto the externally supplied reference.

CAUTION The module can lock onto a signal that is close to the specified reference frequency. If you specify a frequency that is different from what is being supplied, you won't get the right output, and might not get an error.

This softkey is grayed out (inactive) for the External and Device clock source selections.

Preset 10.0000000 MHz

Range 1–100 MHz

SCPI
```
:DIGital:CLOCk:REFerence:FREQuency <val><unit>
:DIGital:CLOCk:REFerence:FREQuency?
```

If this command is executed when the clock source is not set to internal, the parameter value is changed, but it is not used by the signal generator until the

clock source is changed to internal.

Because a query returns the currently set value, regardless of the clock source, you must query both states (reference frequency and clock source) to know the signal generator's current setup.

Rotation

When in Output mode, this softkey enables you to adjust the rotation the IQ constellation for the N5102A module data.

Preset 0.0 deg

Range 0–360 degrees

SCPI
```
:DIGital:DATA:ROTation <val>
:DIGital:DATA:ROTation?
```

Run Loop Back Test

This softkeys starts the selected diagnostic loop back test and returns the results of the test as a pass or fail.

SCPI
```
:DIGital:DIAGnostic:LOOPback? DIGBus|CABLe|N5102A|DEVice
```

This command executes the selected loop back test and returns the results of the test as pass or fail.

Samples

This softkey selects ESG/PSG filtered samples as the baseband data. This is the factory preset data type. When an ARB modulation format is on, this softkey is not accessible.

SCPI
```
:DIGital:DATA:TYPE Samples
:DIGital:DATA:TYPE?
```

If this command is executed while an ARB modulation format is active, the parameter choice is changed, but it is not *used* by the signal generator until a real-time modulation format is turned on.

Because a query returns the current choice, regardless of whether or not an ARB format is active, you must query both states (data type and the modulation format) to know the signal generator's current setup.

Scaling

When in Output mode, this softkey enables you to adjust the scaling of the I and Q data for the N5102A module. This feature is primarily used to remove overrange errors. In Input mode, see "Baseband Setup" on page 88 for information on scaling.

Preset 70.00%

Range -100 to 100%

SCPI
```
:DIGital:DATA:SCALing <val>
:DIGital:DATA:SCALing?
```

Serial

This softkey enables serial data transmission through the N5102A module.

SCPI
```
:DIGital:PCONFig SERial
:DIGital:PCONFig?
```

SigGen Dig Bus

This softkey selects a loop back test that verifies the output capability of the ESG/PSG Digital Bus connector. This test requires the use of the DIG BUS LOOP BACK FIXTURE (supplied with the N5102A module). This is the factory preset loop back test selection. To run the test, see "Run Loop Back Test" on page 101.

SCPI
```
:DIGital:DIAGnostic:LOOPback? DIGBus
```

This command executes the diagnostic test and returns the results of the test as pass or fail.

Signal Type IQ IF

This softkey is applicable for only the output direction with parallel and parallel interleaved data transmissions. The signal type softkey enables you to select the digital signal type for the output of the N5102A module. For a serial port configuration and input mode, this softkey is grayed out (inactive) and IQ shows as the signal type.

IQ The output of the N5102A module is digital IQ data, which is applicable to both parallel/parallel interleaved and serial port configurations.

IF The digital I and Q samples are combined and modulated on an intermediate frequency (IF) carrier. The frequency of the IF (the center frequency of the modulated IF signal) is set to one-fourth of the sample rate (for example, for a 400 MHz clock rate, the IF is 100 MHz). This is available for only the output direction with parallel and parallel interleaved data transmissions.

Preset IQ

SCPI
```
:DIGital:DATA:STYPe IQ|IF
:DIGital:DATA:STYPe?
```

If this command is executed with a serial port configuration, the parameter value is changed, but it is not used by the signal generator until the port configuration is changed to parallel or parallel interleaved.

Because a query returns the currently set value, regardless of the port

configuration, you must query both states (signal type and port configuration) to know the signal generator's current setup.

Swap IQ Off On

This softkey enables and disables the IQ swap feature. When this feature is on, the I data is available on the Q data bus and the Q data is available on the I data bus.

Preset Off

SCPI
```
:DIGital:DATA:IQSWap On|Off|0|1
:DIGital:DATA:IQSWap?
```

Word Alignment

This softkey enables you to align bits when the word size is less than 16 bits. When MSB is selected, the MSB of the data will always be on the same data line and the LSB will move depending on the number of bits in the word. When LSB is selected, the LSB of the data will always be on the same data line and the MSB will move depending on the number of bits in the word. This feature is only available in parallel modes.

Preset MSB

SCPI
```
:DIGital:DATA:ALIGnment MSB|LSB
:DIGital:DATA:ALIGnment?
```

Word Size

This softkey sets the number of bits in each sample transmitted through the N5102A module. A word is defined as an integer number of bits from 4 to 16. For parallel and parallel interleaved data, Word is synonymous with sample. Any unused data lines are driven low.

Preset 16

Range 4–16

SCPI
```
:DIGital:DATA:SIZE <val>
:DIGital:DATA:SIZE?
```

6 Troubleshooting

This chapter provides the following information to assist you in troubleshooting the N5102A Baseband Studio digital signal interface module:

If You Encounter a Problem

CAUTION Immediately unplug the N5102A module from the AC power line if the unit shows any of the following symptoms:

- Smoke, arcing, or unusual noise from inside the unit.
- A circuit breaker or fuse on the main AC power line opens.

These potentially serious faults must be corrected before proceeding.

If the signal generator displays an error, read the error message text by pressing **Utility** > **Error Info**. Resolve any problems specific to the signal generator (refer to the signal generator's documentation).

If the N5102A module is not operating properly, refer to the following table to begin troubleshooting.

Symptom	Action
Power LED is off	Go to "Checking Power Problems" on page 107
Fails "Operation Verification" on page 11	Go to "Running Diagnostic Tests" on page 108
ESG/PSG has a persistent N5102A module error. A module error persists even after you fix the problem described in the error message and clear the error queue: **Utility** > **Error Info** > **Clear Error Queue(s)**	Reset the module (disconnect the power supply from the digital module and then reconnect it).

NOTE If new firmware is downloaded to the ESG/PSG while the digital module is connected, you must power cycle the digital module to restore normal operation. Disconnect the power supply from the digital module and then reconnect it. This will preset the digital module.

Checking Power Problems

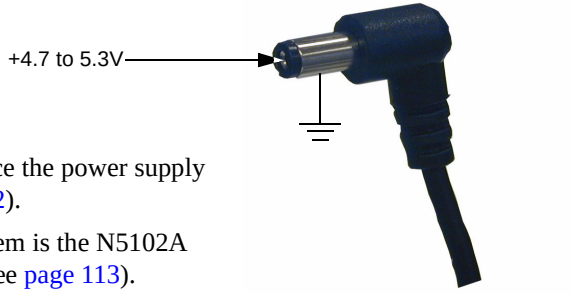
When you connect the power supply to the module, the green Power LED should light.

If the Power LED does not light:

1. Check the power cord; ensure that it is:
   - in good condition
   - properly plugged in to a live outlet (line power connection is described on page 6)
   - properly connected to the power supply (power supply connection is described on page 10) and the DC power supply plug is fully inserted into the N5102A module DC power receptacle

   If this does not solve the problem, go to step 2 to check the power supply.

2. Using a DVM, check the power supply output.

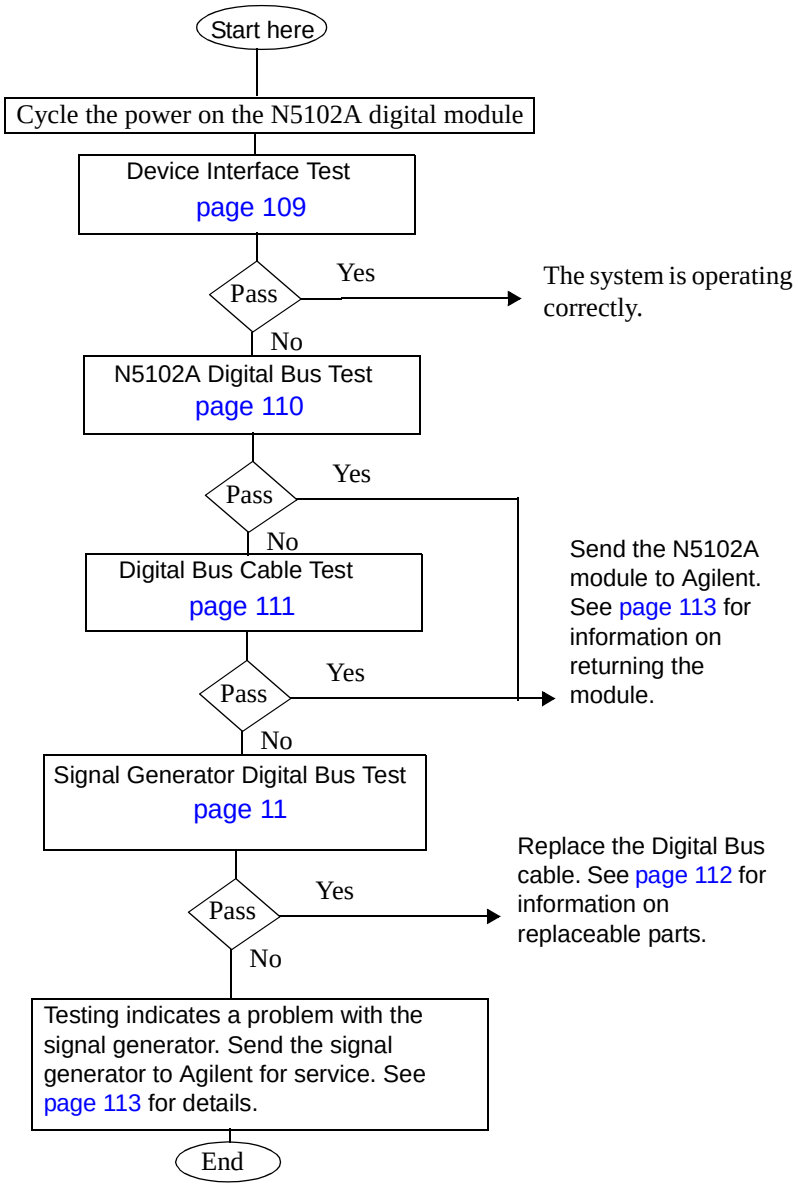


   If the output voltage is not correct, replace the power supply (refer to "Replaceable Parts" on page 112).

   If the output voltage is correct, the problem is the N5102A module. Return the module to Agilent (see page 113).

Running Diagnostic Tests

Diagnostic tests, referred to as loop back tests, are provided to help isolate a problem. Perform the tests, in the order listed, in the following flow chart.



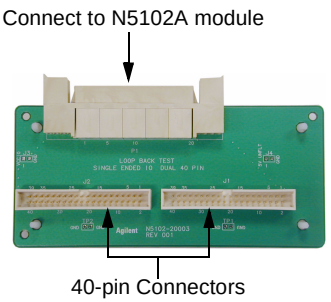
Device Interface (System) Test

This is a comprehensive test that checks the paths from the signal generator Digital Bus connector to the Device Interface connector on the N5102A module. This is the same test used in the section, "Operation Verification" on page 11, which describes the test in more detail.

1. Connect the N5102A module to the signal generator according to the steps in "Connecting the N5102A Module to the ESG/PSG" on page 8.

2. Connect the Loop Back Test Single Ended IO Dual 40 Pin board, shown at right, to the Device Interface connector on the rear of the N5102A module.

   Ensure that there are no connections to the two 40-pin connectors.



3. Select and run the Device Interface test:

   a. On the signal generator, press
   Aux Fctn > **N5102A Interface** > **Diagnostics** > **Loop Back Test Type** > **Device Intfc**.

   Note that the test selection in parentheses below the **Loop Back Test Type** softkey updates to reflect the current test.

   b. Press **Run Loop Back Test**.

   Because all signal generator modulation formats and the N5102A module interface must be off before a loop back test can run, if they are active when you press the **Run Loop Back Test** softkey, they turn off automatically.

Results:

Pass	The system is operating correctly.
Fail	Examine all connectors (they should be clean and undamaged) and connections (they must be secure). If the test still fails, perform the N5102A Digital Bus test to help isolate the problem.

N5102A Digital Bus Test

This test checks the communication path from the Digital Bus connector on the signal generator to the input of the N5102A module. It does not require the use of a loop back test board.

1. If not already done, disconnect the Loop Back Test Single Ended IO Dual 40 Pin board from the N5102A module.

   Leave all other connections.

2. Select and run the N5102A Digital Bus test:

   On the signal generator, press **Loop Back Test Type** > **N5102A Dig Bus** > **Run Loop Back Test**.

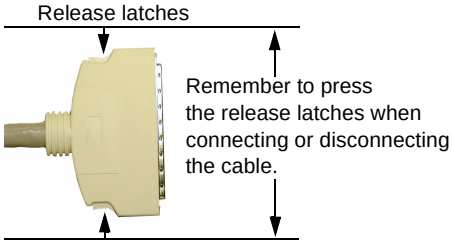
Results:

Pass	The N5102A module has a problem, send the module to Agilent for service (see page 113).
Fail	Perform the Digital Bus Cable test to further isolate the problem.

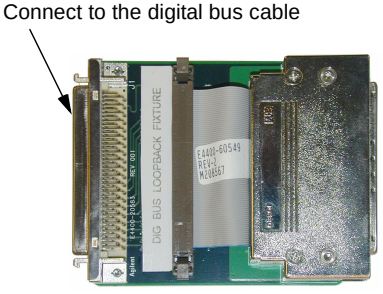
Digital Bus Cable Test

This test checks the communication path from the Digital Bus connector on the signal generator to the end of the digital bus cable. It requires the use of the digital bus loop back fixture.

1. Disconnect the digital bus cable from the N5102A module.



2. Check the connectors on the digital bus loop back fixture, shown at right, to ensure that they are clean and undamaged, then connect it securely to the digital bus cable in place of the module.



3. Select and run the Digital Bus Cable test:

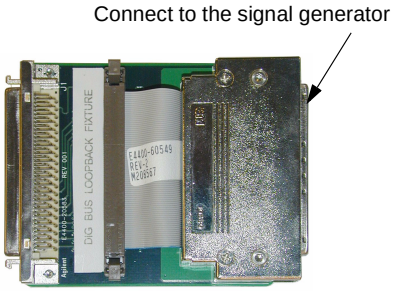
   On the signal generator, press **Loop Back Test Type** > **Dig Bus Cable** > **Run Loop Back Test**.

Results:

Pass	The N5102A module has a problem, send the module to Agilent for service (see page 113).
Fail	Perform the Signal Generator Digital Bus test to further isolate the problem.

Signal Generator Digital Bus Test

This test checks the digital output capability of the signal generator and requires the use of the loop back fixture, shown at right.



1. Disconnect the digital bus loop back fixture from the digital bus cable.
2. Disconnect the digital bus cable from the signal generator, and connect the digital bus loop back fixture securely in its place.
3. Select and run the Signal Generator Digital Bus test

   On the signal generator, press **Loop Back Test Type** > **SigGen Dig Bus** > **Run Loop Back Test**.

Results:

Pass	The problem is with the digital bus cable; replace the cable (see "Replaceable Parts" on page 112).
Fail	The problem is with the signal generator; send the signal generator to Agilent for service (see page 113).

Replaceable Parts

Contact Agilent (see Table 6-1) for price and availability of the following parts.

Description	Part Number	Description	Part Number
Digital Bus Cable	N5101-60003	Power Cord	
Digital Bus Loop Back Fixture	E4400-63583	United Kingdom	8120-8709
Loop Back Test Single Ended IO Dual 40 Pin Board	N5102-63003	Australia and New Zealand	8120-0696
Single Ended I/O Dual 20 Pin Board	N5102-63004	Continental Europe	8120-1692
Differential I/O 38 Pin Board	N5102-63005	United States and Canada, 120V	8120-1521
Differential I/O Dual 100 Pin Board	N5102-63006	Switzerland	8120-2296
Single Ended I/O 68 Pin Board	N5102-63007	Denmark	8120-2957
N5102A User’s Guide	N5102-90001	South Africa and India	8120-4600
Documentation CD	N5102-90002	Japan	8120-4754
Power Supply, AC-DC 5V 4A	0950-4540	Israel	8120-5181
		Argentina	8120-6868
		Chile	8120-6979
		China	8120-8377
		Brazil and Thailand	8120-8671

Returning an Instrument to Agilent Technologies

1. Be prepared to give the service representative as much information as possible regarding the instrument's problem, and all the information found on the instrument's serial tag.
2. Either use the URL listed in Table 6-1 to locate your key contact, or call the phone number listed below that is appropriate to the instrument's location. After providing information about the instrument and the problems you are experiencing, you will receive instructions on where to ship the instrument for repair.
3. If they are available, use the original factory packaging materials. If not, use similar packaging to properly protect the instrument.

Table 6-1 Contacting Agilent

Online assistance: `www.agilent.com/find/assist`			
United States (tel) 1 800 452 4844	**Latin America** (tel) (305) 269 7500 (fax) (305) 269 7599	**Canada** (tel) 1 877 894 4414 (fax) (905) 282-6495	**Europe** (tel) (+31) 20 547 2323 (fax) (+31) 20 547 2390
New Zealand (tel) 0 800 738 378 (fax) (+64) 4 495 8950	**Japan** (tel) (+81) 426 56 7832 (fax) (+81) 426 56 7840	**Australia** (tel) 1 800 629 485 (fax) (+61) 3 9210 5947	

Asia Call Center Numbers

Country	Phone Number	Fax Number
Singapore	1-800-375-8100	(65) 836-0252
Malaysia	1-800-828-848	1-800-801664
Philippines	(632) 8426802 1-800-16510170 (PLDT Subscriber Only)	(632) 8426809 1-800-16510288 (PLDT Subscriber Only)
Thailand	(088) 226-008 (outside Bangkok) (662) 661-3999 (within Bangkok)	(66) 1-661-3714
Hong Kong	800-930-871	(852) 2506 9233
Taiwan	0800-047-866	(886) 2 25456723
People's Republic of China	800-810-0189 (preferred) 10800-650-0021	10800-650-0121
India	1-600-11-2929	000-800-650-1101

Numerics

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